SAMSUNG

Rev. 1.3, May. 2024

MZWL6960HFJA-00B07
MZWL61T9HFLT-00B07
MZWL63T8HFLT-00B07
MZWL67T6HBLC-00B07
MZWL615THBLF-00B07

SAMSUNG SSD PM9D3a

Specification(PCIe® NVMe™ U.2)

Datasheet

IF THERE IS ANY OTHER OPERATION TO IMPLEMENT IN ADDITION TO SPECIFICATION IN THE DATASHEET OR JEDEC STANDARD, PLEASE CONTACT EACH BRANCH OFFICE OR HEADQUARTERS OF SAMSUNG ELECTRONICS.

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Revision History

No.	Description	Date	Remark	Editor	Reviewed by
1.0	1. Initial issue	Sep. 26, 2023	Final	Semi Lee	Changyoung CHA
1.1	1. LBA Count of 15.36TB in table2: IDEMA rule → SFF-8447 rule	Jan. 29, 2024	Final	Semi Lee	Changyoung CHA
1.2	1. 960GB, 1.92TB and 3.84TB added.	Mar. 14, 2024	Final	Semi Lee	Changyoung CHA
1.3	1. ch8.3 Vital Product Data(VPD) Structure added.	May. 29, 2024	Final	Semi Lee	Changyoung CHA

Part Number	Capacity[1)]	LBA Count
MZWL6960HFJA-00B07	960GB	1,875,385,008
MZWL61T9HFLT-00B07	1.92TB	3,750,748,848
	1.6TB	3,125,627,568
MZWL63T8HFLT-00B07	3.84TB	7,501,476,528
	3.2TB	6,251,233,968
MZWL67T6HBLC-00B07	7.68TB	15,002,931,888
	6.4TB	12,502,446,768
MZWL615THBLF-00B07	15.36TB	30,001,856,512
	12.8TB	25,000,148,992

FEATURES

· PCI Express® Gen.5
  - PCI Express® CEM Specification Rev. 5.0
  - PCI Express® Base Specification Rev. 5.0
  - NVM Express™ Specification Rev. 2.0
  - Single port x4 lanes
· Enhanced Power-Loss Data Protection
· End-to-End Data Protection
· Support SSD Enhanced S.M.A.R.T. Feature Set
· Hardware based AES-XTS 256-bit Encryption Engine
· Static and Dynamic Wear Leveling
· RoHS / Halogen-Free Compliant
· TCG Opal Compliant

DRIVE CONFIGURATION

· Form Factor	2.5" U.2
· Interface	PCI Express® Gen.5 x4
· Bytes per Sector	512, 520, 4096, 4160 Bytes

PERFORMANCE SPECIFICATIONS[2)]

· Gen.5

· Data Transfer Rate (128KB data size)

- Sequential Read[3)]	Up to 12,000 MB/s
- Sequential Write[3)]	(960GB) Up to 1,500 MB/s (1.92/ 1.6TB) Up to 3,300 MB/s (3.84/ 3.2TB) Up to 6,700 MB/s (7.68/ 15.36/ 6.4/ 12.8TB) Up to 7,000 MB/s

· Data I/O Speed (4KB data size, Sustained)

- Random Read	(960GB) Up to 950K IOPS (1.92/ 1.6TB) Up to 1,500K IOPS (3.84/ 7.68/ 3.2TB) Up to 1,700K IOPS (15.36/ 6.4/ 12.8TB) Up to 1,800K IOPS
- Random Write	(960GB) Up to 70K IOPS (1.92TB) Up to 150K IOPS (3.84TB) Up to 250K IOPS (7.68/ 15.36TB) Up to 400K IOPS (1.6TB) Up to 360K IOPS (3.2TB) Up to 610K IOPS (6.4TB) Up to 700K IOPS (12.8TB) Up to 710K IOPS

· Latency (Sustained workload)

- Random Read/ Write (typical)[4)]	(1.6/ 3.2TB) Up to 60/9 us (960GB/ 1.92/ 3.84/ 7.68/ 15.36/ 6.4/ 12.8TB) Up to 65/9 us
- Sequential Read/ Write (typical)[5)]	Up to 9/9 us
- Drive Ready Time (typical)	(960GB/ 1.92/ 3.84/ 1.6/ 3.2TB) Up to 8 s (7.68/ 6.4TB) Up to 11 s (15.36/ 12.8TB) Up to 13 s

RELIABILITY SPECIFICATIONS

· Uncorrectable Bit Error Rate	1 sector per 10^{17} bits read
· MTBF	2,500,000 hours
· Component Design Life	5 years
· Endurance (JEDEC Workload)	
- 960GB/1.92TB/3.84TB/7.68TB/15.36TB	1 DWPD
- 1.6TB/3.2TB/6.4TB/12.8TB	3 DWPD
· TBW (JEDEC Workload)	
- 960GB	1,752TB
- 1.92TB	3,504TB
- 1.6TB	8,760TB
- 3.84TB	7,008TB
- 3.2TB	17,520TB
- 7.68TB	14,016 TB
- 15.36TB	28,032 TB
- 6.4TB	35,040 TB
- 12.8TB	70,080 TB
· Data Retention	3 months

ENVIRONMENTAL SPECIFICATIONS

· Temperature[6)]	
- Operating	0 ~ 70 °C
- Non-operating	-40 ~ 85 °C
· Humidity (non-condensing)	5 ~ 95%
· Linear Shock (0.5ms duration with 1/2 sine wave)	
- Non-operating	1,500 G
· Vibration (20 ~ 2,000 Hz, Sinusoidal)	
- Non-operating	20G

POWER REQUIREMENTS

· Supply Voltage / Tolerance	12V±10%
· Gen.5	
- Active (max. RMS)	Up to 16.4 W
- Idle (typ.)[7)]	Up to 4.3 W
· Gen.4	
- Active (max. RMS)	Up to 15.1 W
- Idle (typ.)[7)]	Up to 3.5 W

PHYSICAL DIMENSION

· Width	69.85 ± 0.25 mm
· Length	100.20 ± 0.25 mm
· Height	15.0+0.00/-0.50 mmT
· Weight	Up to 170 g

· **Gen.4**

· Data Transfer Rate (128KB data size)

- Sequential Read[3)] (960GB/ 1.6TB) Up to 6,400 MB/s
  (3.2TB) Up to 6,500 MB/s
  (1.92/ 3.84/ 7.68/ 15.36/ 6.4/ 12.8TB) Up to 7,000 MB/s

- Sequential Write[3)] (960GB) Up to 1,400 MB/s
  (1.92/ 1.6TB) Up to 3,100 MB/s
  (3.84/ 7.68/ 15.36/ 3.2/ 6.4/ 12.8TB) Up to 4,100 MB/s

· Data I/O Speed (4KB data size, Sustained)

- Random Read (960GB) Up to 950K IOPS
  (1.92TB) Up to 1,000K IOPS
  (3.84/ 7.68/ 15.36TB) Up to 1,100K IOPS
  (1.6/ 3.2/ 6.4/ 12.8TB) Up to 1,200K IOPS

- Random Write (960GB) Up to 70K IOPS
  (1.92TB) Up to 150K IOPS
  (3.84/ 7.68/ 15.36TB) Up to 200K IOPS
  (1.6TB) Up to 240K IOPS
  (3.2/ 6.4/ 12.8TB) Up to 250K IOPS

· Latency (Sustained workload)

- Random Read/ Write (typical)[4)] (1.6/ 3.2TB) Up to 60/9 us
  (960GB/ 1.92/ 3.84/ 7.68/ 15.36/ 6.4/ 12.8TB) Up to 65/9 us
- Sequential Read/ Write (typical)[5)] Up to 9/9 us
- Drive Ready Time (typical) (960GB/ 1.92/ 3.84/ 1.6/ 3.2TB) Up to 8 s
  (7.68/ 6.4TB) Up to 11 s
  (15.36/ 12.8TB) Up to 13 s

***NOTE:** Specifications are subject to change without notice.*

1) 1GB = 10^9 Bytes, 1TB = 10^{12} Bytes, unformatted Capacity.
User accessible capacity may vary depending on operating environment and formatting.
2) Based on PCI Express Gen5x4, Random performance measured using FIO 3.32 in Linux CentOS8(Kernel 5.19) with 4KB (4,096 bytes) of data transfer size in queue depth 64 by 4 workers and Sequential performance with 128KB (131,072 bytes) of data transfer size in queue depth 256 by 1 worker. Actual performance may vary depending on use conditions and environment.
3) 1 MB/sec = 1,000,000 bytes/sec was used in sequential performance.
4) The random latency is measured by using FIO 3.32 in Linux CentOS8(Kernel 5.19) and 4KB (4,096 bytes) transfer size with queue depth 1 by 1 worker.
5) The Sequential latency is measured by using FIO 3.32 in Linux CentOS8 (Kernel 5.19) and 4KB (4,096 bytes) transfer size with queue depth 1 by 1 worker.
6) Temperature indicates Case temperature (Tcase(Tc)) at the hottest point on the case. Sufficient cool/warm conditions is highly recommended to operate properly within the operating temperature range.
7) Idle power is measured at 35°C Temperature

Table Of Contents

1.0 INTRODUCTION

1.1 General Description

This document describes the specifications of the Samsung SSD PM9D3a, which is a native-PCIe® SSD for enterprise application.

The Samsung SSD PM9D3a presents outstanding performance with instant responsiveness to the host system, by applying the Peripheral Component Interconnect Express (PCIe®) 5.0 interface standard, as well as highly efficient Non-Volatile Memory Express (NVMe™) Protocol.

The Samsung SSD PM9D3a delivers wide bandwidth of up to 12,000MB/s for sequential read speed and up to 7,000MB/s for sequential write speed under up to 16.4W power.
With the help of Toggle 4.0 NAND Flash interface, the Samsung SSD PM9D3a delivers random performance of up to 1,800KIOPS for random 4KB read and up to 400KIOPS for random 4KB write in the sustained state.

By combining the enhanced reliability Samsung NAND Flash memory silicon with NAND Flash management technologies, the Samsung SSD PM9D3a delivers the extended endurance of up to 1 drive writes per day over 5 years, which is suitable for enterprise applications
In addition, the Samsung SSD PM9D3a supports Power Loss Protection (PLP).
PLP solution can guarantee that data issued by the host system are written to the storage media without any loss in the event of sudden power off or sudden power failure.

1.2 Product List

[Table 1] Product List

Type	Capacity	Part Number
U.2[1)]	960GB	MZWL6960HFJA-00B07
	1.92TB	MZWL61T9HFLT-00B07
	1.6TB	
	3.84TB	MZWL63T8HFLT-00B07
	3.2TB	
	7.68TB	MZWL67T6HBLC-00B07
	6.4TB	
	15.36TB	MZWL615THBLF-00B07
	12.8TB	

1.3 Ordering Information

M Z X X X X X X X X X X - X X X X X

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

1. Memory (M)

2. Module Classification
Z: SSD

3. Form Factor
W: PCIe® 2.5 inch

4. Line-Up
L: VNAND 3bit MLC

5. SSD CTRL
6: Deneb

6~8. SSD Density
960: 960GB
1T9: 1.92TB
3T8: 3.84TB
7T6: 7.68TB
15T: 15.36TB

9. NAND PKG + NAND Voltage
H: BGA (LF,HF)

10. Flash Generation
B: 3rd Generation
F: 7th Generation

11~12. NAND Density
LC: 8T ODP 2CE
LF: 16T HDP 2CE
LT: 4T ODP 2CE
JA: 2T QDP 2CE

13. "-"

14. Default
"0"

15. HW revision
0: No revision

16. Packaging type
B: Bulk Packing with production from both Korea & China

17~18. Customer
07: General

2.0 PRODUCT SPECIFICATIONS

2.1 Capacity

[Table 2] User Capacity and Addressable Sectors

Capacity[1)2)]	LBA Count[3)]
960GB	1,875,385,008
1.92TB	3,750,748,848
1.6TB	3,125,627,568
3.84TB	7,501,476,528
3.2TB	6,251,233,968
7.68TB	15,002,931,888
6.4TB	12,502,446,768
15.36TB	30,001,856,512
12.8TB	25,000,148,992

NOTE:
1) 1GB = 10^9 Bytes, 1TB = 10^{12} Bytes, 1 Sector = 512Bytes
2) Capacity shown in Table 2 represents the total usable capacity of the SSD which may be less than the total physical capacity.
A certain area in physical capacity, not in the area shown to the user, might be used for the purpose of NAND flash management.
3) LBA Count shown in Table 2 represents the total user addressable sectors in LBA mode.
960GB~7680GB is calculated by IDEMA rule and 12.8TB/15.36TB is calculated by SFF-8447 rule.

2.2 Performance

[Table 3] Sustained Random Read/Write Performance (IOPS)

Maximum Performance[1)]		Unit	960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
PCIe® Gen.4	Random 4KB Read (Up to)	IOPS	950K	1000K	1100K	1100K	1100K	1200K	1200K	1200K	1200K
	Random 4KB Write (Up to)	IOPS	70K	150K	200K	200K	200K	240K	250K	250K	250K
PCIe® Gen.5	Random 4KB Read (Up to)	IOPS	950K	1500K	1700K	1700K	1800K	1500K	1700K	1800K	1800K
	Random 4KB Write (Up to)	IOPS	70K	150K	250K	400K	400K	360K	610K	700K	710K

NOTE:
1) Random performance in Table 3 was measured by using FIO 3.32 in Linux CentOS8(Kernel 5.19) with 4KB(4,096 bytes) of data transfer size in Queue Depth=64 by 4 workers. Measurements were performed on a full Logical Block Address (LBA) span of the drive in sustained state. The actual performance may vary depending on use conditions and environment.

[Table 4] Sequential Read/Write Performance

Maximum Performance[1)]		Unit	960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
PCIe® Gen.4	Sequential 128KB Read (Up to)	MB/s	6400	7000	7000	7000	7000	6400	6500	7000	7000
	Sequential 128KB Write (Up to)	MB/s	1400	3100	4100	4100	4100	3100	4100	4100	4100
PCIe® Gen.5	Sequential 128KB Read (Up to)	MB/s	12000	12000	12000	12000	12000	12000	12000	12000	12000
	Sequential 128KB Write (Up to)	MB/s	1500	3300	6700	7000	7000	3300	6700	7000	7000

NOTE:
1) Sequential performance in Table 4 was measured by using FIO 3.32 in Linux CentOS8(Kernel 5.19) with 128KB (131,072 bytes) of data transfer size in Queue Depth=256 by1 worker.

[Table 5] IOPS Consistency

Maximum Performance[1)]	960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
Random Read (4 KB)[2)]	95%	95%	95%	95%	95%	95%	95%	95%	95%
Random Write (4 KB)	95%	95%	95%	95%	95%	95%	95%	95%	95%

NOTE:
1) IOPS consistency measured using FIO with queue depth 256.
2) IOPS Consistency (%) = (99.9% IOPS) / (Average IOPS) x 100.

2.3 Latency

[Table 6] Latency[1] (sustained state)

Queue Depth = 1	Unit	960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
Random Read/Write[2]	us	65/9	65/9	65/9	65/9	65/9	60/9	60/9	65/9	65/9
Sequential Read/Write[3]	us	9/9								
Drive Ready Time[4]	sec	8	8	8	11	13	8	8	11	13

NOTE:
1) Typical values (P50)
2) The random latency is measured by using FIO 3.32 in Linux CentOS8(Kernel 5.19) - Gen.5 and 4KB transfer size with queue depth 1 by 1 worker.
3) The sequential latency is measured by using FIO 3.32 in Linux CentOS8(Kernel 5.19) - Gen.5 and 4KB transfer size with queue depth 1 by 1 worker.
4) The maximum taking time to be ready for receiving commands after power-up (CSTS.Ready=1). It is expected that I/O commands may not be completed at this point.

2.4 Quality of Service (QoS)

[Table 7] Quality of Service (QoS)[1]

Quality of Service (99%)[2]	Unit	960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
Read(4KB, QD=1)	ms	0.08	0.08	0.08	0.090	0.090	0.08	0.08	0.090	0.090
Read(4KB, QD=32)	ms	0.2	0.16	0.13	0.150	0.150	0.15	0.13	0.150	0.150
Write(4KB, QD=1)	ms	0.015	0.01	0.01	0.015	0.015	0.01	0.01	0.015	0.015
Write(4KB, QD=32)	ms	0.5	0.25	0.15	0.160	0.160	0.15	0.13	0.160	0.160

Quality of Service (99.99%)[3]	Unit	960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
Read(4KB, QD=1)	ms	0.1	0.08	0.08	0.090	0.090	0.08	0.08	0.090	0.090
Read(4KB, QD=32)	ms	0.35	0.25	0.2	0.210	0.210	0.25	0.2	0.210	0.210
Write(4KB, QD=1)	ms	0.02	0.01	0.01	0.015	0.015	0.01	0.01	0.015	0.015
Write(4KB, QD=32)	ms	0.45	0.23	0.16	0.210	0.210	0.18	0.15	0.210	0.210

NOTE:
1) QoS is measured using FIO 3.32 in Linux CentOS8(Kernel 5.19) - Gen.5(99 and 99.99%) with queue depth 1, 32 on 4KB random read and write.
2) QoS is measured as the maximum round-trip time taken for 99 and 99.99% of commands to host.
3) QoS is measured as the maximum round-trip time taken for 99.99 % of commands to host.

2.5 Power

The Samsung SSD PM9D3 is implemented in standardized U.2 form factor and gets primary 12V power from the host system.
For 12V, the allowable voltage tolerance and noise level in SSD are described in chapter 2.5.1, the power consumption in chapter 2.5.2 and the inrush current in chapter 2.5.3.

2.5.1 Operating Voltage (12V and 3.3Vaux)

[Table 8] Operating Voltage Conditions[1]

Operating Voltage	960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
12V	12V±10%								
12V Noise Level	DC to 100Khz: 450mVp-p Max 100Khz to 220Mhz: 350mVp-p Max								
12V Rise Time (Max/Min)	1s/1ms								
12V Fall Time (Max/Min)	1s/1ms								
12V Minimum Off Time	10ms								
3.3Vaux	3.3V±15%								

NOTE:
1) The components inside SSD were designed to endure the range of voltage fluctuations, which might be induced by the host system.

2.5.2 Power Consumption (12V)

[Table 9] Power Consumption (12V Supply Voltage)[1)]

Power Mode			960GB	1.92TB/1.6TB	3.84TB/3.2TB	7.68TB/6.4TB	15.36TB/12.8TB
PCIe® Gen.4	Active	Read	8.0 W	10.0 W	11.0 W	12.2 W	13.0 W
		Write	7.3 W	10.3 W	14.8 W	14.9 W	15.1 W
	Idle[2)]		3.1 W	3.2 W	3.2 W	3.3 W	3.5 W
PCIe® Gen.5	Active	Read	11.0 W	11.2 W	12.8 W	13.5 W	14.1 W
		Write	8.1 W	11.1 W	15.6 W	16.3 W	16.4 W
	Idle[2)]		3.9 W	4.0 W	4.0 W	4.3 W	4.3 W

NOTE:
1) Typical Power Consumption (Maximum average power with a measurement period of 1s)
2) Idle power is measured at 35°C Temperature

2.5.3 Inrush Current

[Table 10] Inrush Current

Inrush Current	960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
12V	1.8A[1)]								

NOTE:
1) The measurement value of inrush current is also compatible with the standard specification of “Enterprise SSD Form Factor Version 1.0a” released by SSD Form Factor Working Group.

2.5.4 Power Loss Protection

By using internal back-up power technology, the Samsung SSD PM9D3 supports power loss protection (PLP) feature to guarantee the reliability of data requested by the host system. When power is unpredictably lost, SSD can detect automatically this abnormal situation and transfer all user data and meta-data cached in DRAM into the Flash media during any SSD operations.

2.6 Reliability

The reliability specification of the Samsung SSD PM9D3 follows JEDEC standard, which are included in JESD218A and JESD219A documents

2.6.1 Mean Time Between Failures

By definition, Mean Time between Failures (MTBF) is the estimated time between failures occurring during SSD operation.

[Table 11] MTBF Specifications

Parameter	960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
MTBF	2,500,000 Hours								

2.6.2 Uncorrectable Bit Error Rate

By definition, Uncorrectable Bit Error Rate (UBER) is a metric for the rate of occurrence of data errors, equal to the number of data errors per bits read as specified in the JESD218A document of JEDEC standard.

[Table 12] UBER Specifications

Parameter	960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
UBER	1 sector per 10^{17} bits read								

NOTE:
1) For the enterprise application, JEDEC recommends that UBER shall be below 10^{-16}

2.6.3 Data Retention

By definition, data retention is the expected time period for retaining data in the SSD at the maximum rated endurance in power-off state as specified in the JESD218A document of JEDEC standard.

[Table 13] Data Retention

Parameter	960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
Data Retention[1)]	3 months								

NOTE:
1) Data retention was measured by assuming that SSD reaches the maximum rated endurance at 40°C in power-off state.

2.6.4 Endurance

By definition, the endurance of SSD in enterprise application is defined as the maximum number of drive writes per day that can meet the requirements specified in the JESD218A and JESD219A (Enterprise endurance workload) document of JEDEC standard.

[Table 14] Drive Write Per Day (DWPD)

Parameter	960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
DWPD	1 drive writes per day over 5years					3 drive writes per day over 5years			

[Table 15] Total Byte Written (TBW)

Parameter	Unit	960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
TBW	TB	1,752	3,504	7,008	14,016	28,032	8,760	17,520	35,040	70,080

2.7 Environmental Specification

2.7.1 Temperature

[Table 16] Stadard Temperatures

Parameter		960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
Temperature[1)]	Operating[1)]	0 to 70°C								
	Non-operating[2)]	-40 to 85°C								

NOTE:
1) Operating Temperature implies Case temperature (Tcase(Tc)) at the hottest point on the case.
Sufficient cool/warm conditions is highly recommended to operate properly within the operating temperature range.
2) Non-Operating temperature implies stroage or shippment.

2.7.2 Humidity

[Table 17] Humidity

Parameter		960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
Humidity[1)]	Non-operating	5% to 95%								

NOTE:
1) Humidity is measured in non-condensing state.

2.7.3 Shock and Vibration

[Table 18] Shock and Vibration

Parameter		960GB	1.92TB	3.84TB	7.68TB	15.36TB	1.6TB	3.2TB	6.4TB	12.8TB
Shock[1)]	Non-operating	1,500G (0.5ms duration with half sine wave)								
Vibration[1)2)]	Non-operating	20G (20 ~ 2,000 Hz, Sinusoidal)								

NOTE:
1) Shock or Vibration specifications assume that SSD shall be mounted with screws when input (shock and vibration) is applied.
The input may be applied in 3 axes (x, y and z).
2) Vibration specifications assume that SSD shall be mounted with screws when input vibration is applied.
The input vibration may be applied in 3 axes (x, y and z) and 4min/cycle, 4cycle/axis on 3 axis.

2.7.3.1 Dynamic Thermal Throttling

The dynamic thermal throttling (DTT) is implemented to prevent overheating. Table 19 shows the engaging thresholds for DTT.

[Table 19] DTT Table

DTT Threshold[1)]	960GB	1.92TB/1.6TB	3.84TB, 3.2TB	7.68TB, 6.4TB, 15.36TB, 12.8TB	Throttled Performance[2)]
DTT1	77°C	77°C	77°C	77°C	< 75%
DTT2	79°C	79°C	79°C	81°C	< 50%
DTT3	81°C	81°C	81°C	83°C	< 25%
Critical (DTT4)	85°C	85°C	85°C	85°C	< 1%
Shut-down[3)]	95°C	95°C	95°C	95°C	n/a
Warning Composite Temperature (WCTEMP)	77°C				
Critical Composite Temperature (CCTEMP)	85°C				

NOTE:
1) All temperatures are based on the composite temperatures (Tcomp).
2) Throttling level could vary with workloads and capacities.
3) Recoverable by normal power off recovery (NPOR).

2.7.3.2 Composite Temperature (Tcomposite; Tcomp)

[Table 20] Tcomp is defined by the correlation equation as follows:

960GB	1.92TB/1.6TB	3.84TB, 3.2TB	7.68TB, 6.4TB, 15.36TB, 12.8TB
Tcomposite = External T/S - 6 (External Sensor ≤ 83)	Tcomposite = External T/S - 6 (External Sensor ≤ 83)	Tcomposite = External T/S - 5 (External Sensor ≤ 82)	Tcomposite = TS - 5 (TS < 82)
Tcomposite = 2* (External T/S - 83) + 77 (83 < External Sensor ≤ 87)	Tcomposite = 2* (External T/S - 83) + 77 (83 < External Sensor ≤ 87)	Tcomposite = 2 * (External T/S - 82) + 77 (82 < External Sensor ≤ 86)	Tcomposite = 2 * TS - 87 (82 ≤ TS < 86)
Tcomposite = (10/7) * (External T/S - 87) + 85 (87 < External Sensor ≤ 94)	Tcomposite = (10/7) * (External T/S - 87) + 85 (87 < External Sensor ≤ 94)	Tcomposite = (10/9) * (External T/S - 95) + 95 (86 < External Sensor ≤ 95)	Tcomposite = 1.25 * TS - 22.5 (86 ≤ TS ≤ 94)

(TS: raw value of thermal sensor on the drive)

3.0 MECHANICAL SPECIFICATIONS

3.1 Physical Information

Enclosure of the Samsung SSD PM9D3 in U.2 form factor follows the standardized dimensions defined by SNIA SFF-TA-1006 SPEC

[Table 21] Physical Dimensions and Weightnical Outline

Parameter	Unit	960GB/ 1.92TB/ 1.6TB/ 3.84TB/ 3.2TB/ 7.68TB/ 15.36TB/ 6.4TB/ 12.8TB
Width	mm	69.85 ± 0.25
Length	mm	100.20 ± 0.25
Height	mm	15.00+0.00/-0.50
Weight	g	Up to 170.0g

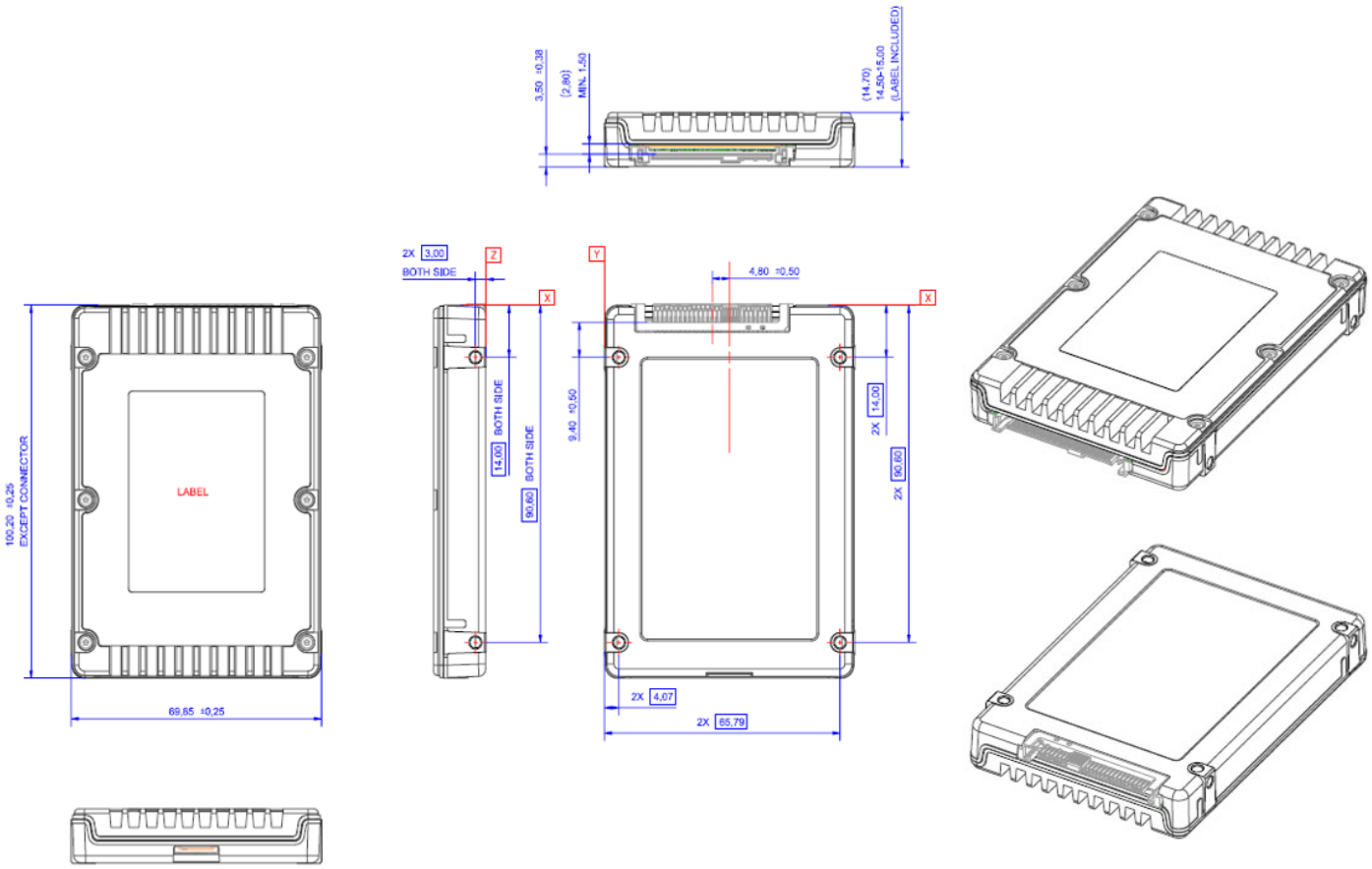
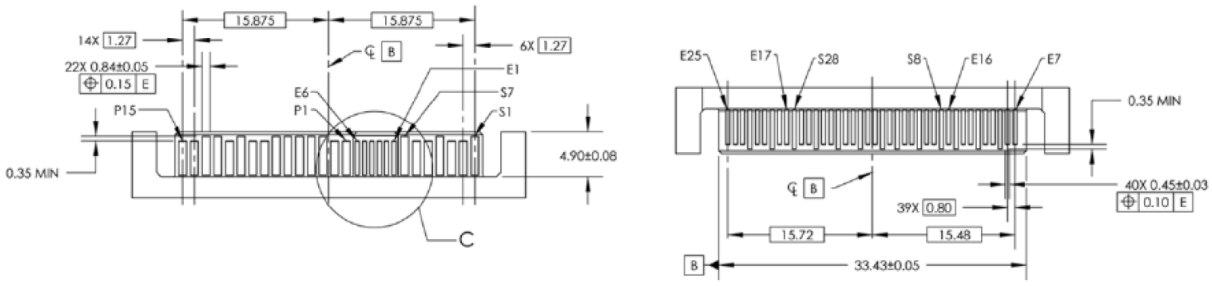


Figure 1. Mechanical Outline

4.0 INTERFACE SPECIFICATION

4.1 Connector Dimensions



4.2 Connector Pin Assignments

[Table 22] Certifications and Declarations

Pin #	Assignment	Description	Pin #	Assignment	Description
S1	GND	Ground	E13	PERn0[1)]	PCIe® Receive- (lane 0)
S2	Not Used	NC (Not connected)	E14	PERp0[1)]	PCIe® Receive+ (lane 0)
S3	Not Used	NC (Not connected)	E15	GND	Ground
S4	GND	Ground	E16	Not Used	NC (Not connected)
S5	Not Used	NC (Not connected)	S8	GND	Ground
S6	Not Used	NC (Not connected)	S9	Not Used	NC (Not connected)
S7	GND	Ground	S10	Not Used	NC (Not connected)
E1	REFCLKB+	Ground	S11	GND	Ground
E2	REFCLKB-	Ground	S12	Not Used	NC (Not connected)
E3	3.3V AUX	3.3V Auxiliary Power	S13	Not Used	NC (Not connected)
E4	CLKREQ#	Clock Request	S14	GND	Ground
E5	PERST#	PCIe® Reset	S15	Not Used	NC (Not connected)
E6	Not Used	NC (Not connected)	S16	GND	Ground
P1	WAKE#	NC (Not connected)	S17	PETp1[1)]	PCIe® Transmit- (lane 1)
P2	Not Used	NC (Not connected)	S18	PETn1[1)]	PCIe® Transmit+ (lane 1)
P3	PWRDIS	Power Disable	S19	GND	Ground
P4	IfDet#	Ground	S20	PERn1[1)]	PCIe® Receive- (lane 1)
P5	GND	Ground	S21	PERp1[1)]	PCIe® Receive+ (lane 1)
P6	GND	Ground	S22	GND	Ground
P7	Not Used	P7, P8 and P9 are tied together	S23	PETp2[1)]	PCIe® Transmit+ (lane 2)
P8	Not Used	P7, P8 and P9 are tied together	S24	PETn2[1)]	PCIe® Transmit- (lane 2)
P9	Not Used	P7, P8 and P9 are tied together	S25	GND	Ground
P10	PRSNT#	NC (Not connected)	S26	PERn2[1)]	PCIe® Receive+ (lane 2)
P11	ACTIVITY#	Device Activity	S27	PERp2[1)]	PCIe® Receive- (lane 2)
P12	GND	Ground	S28	GND	Ground
P13	12V Precharge	12V Precharge Power	E17	PETp3[1)]	PCIe® Transmit+ (lane 3)
P14	12V	12V Primary Power	E18	PETn3[1)]	PCIe® Transmit- (lane 3)
P15	12V	12V Primary Power	E19	GND	Ground
E7	REFCLK+	PCIe® Reference Clock +	E20	PERn3[1)]	PCIe® Receive- (lane 3)
E8	REFCLK-	PCIe® Reference Clock -	E21	PERp3[1)]	PCIe® Receive- (lane 3)
E9	GND	Ground	E22	GND	Ground

E10	PETp0[1)]	PCIe® Transmit- (lane 0)	E23	SMBCLK	SMBus Clock
E11	PETn0[1)]	PCIe® Transmit+ (lane 0)	E24	SMBDAT	SMBus Data
E12	GND	Ground	E25	DualPortEn#	NC (Not connected)

NOTE:

1) Names on the pin assignments and description are written from the PCIe® host system/platform perspective.
The PETpx and PETnx pins shall be connected to the PCI Express® Transmitter differential pair on the host system/platform board.
The PERpx and PERnx pins shall be connected to the PCI Express® Receiver differential pair on host system/platform board.

2) Support for Lane Polarity Inversion is required on PCIe® Receivers across all Lanes independently.

5.0 PCI and NVM EXPRESS REGISTERS

5.1 PCI Express® Registers

5.1.1 PCI Register Summary

[Table 23] PCI Register Summary

Start Address	End Address	Name	Type
00h	3Fh	PCI Header	PCI Configuration Header Space
40h	47h	PCI Power Management Capability	PCI Capability
50h	67h	MSI Capability	PCI Capability
70h	A3h	PCI Express® Capability	PCI Capability
B0h	BBh	MSI-X Capability	PCI Capability
100h	12Bh	Advanced Error Reporting (AER) Capability	PCI Extended Capability
168h	17Bh	Secondary PCI Express® Capability	PCI Extended Capability
188h	1ABh	Physical Layer 16.0 GT/s Capability	PCI Extended Capability
1ACh	1C3h	Margining Extended Capability Header	PCI Extended Capability
364h	36Fh	Data Link Feature Extended Capability	PCI Extended Capability

5.1.2 PCI Header Registers

[Table 24] PCI Header Register Summary

Start Address	End Address	Symbol	Description
00h	03h	ID	Identifiers
04h	05h	CMD	Command Register
06h	07h	STS	Device Status
08h	08h	RID	Revision ID
09h	0Bh	CC	Class Codes
0Ch	0Ch	CLS	Cache Line Size
0Dh	0Dh	MLT	Master Latency Timer
0Eh	0Eh	HTYPE	Header Type
0Fh	0Fh	BIST	Built in Self Test
10h	13h	MLBAR (BAR0)	Memory Register Base Address (lower 32-bit)
14h	17h	MUBAR (BAR1)	Memory Register Base Address (upper 32-bit)
18h	1Bh	IDBAR (BAR2)	Index/Data Pair Register Base Address
1Ch	1Fh	BAR3	Reserved
20h	23h	BAR4	Reserved
24h	27h	BAR5	Reserved
28h	2Bh	CCPTR	CardBus CIS Pointer
2Ch	2Fh	SS	Subsystem Identifiers
30h	33h	EROM	Expansion ROM Base Address
34h	34h	CAP	Capabilities Pointer
35h	3Bh	RO	Reserved
3Ch	3Dh	INTR	Interrupt Information
3Eh	3Eh	MGNT	Minimum Grant
3Fh	3Fh	MLAT	Maximum Latency

[Table 25] Identifier Register

Bits	Type	Default Value	Description
31:16	RO	A80Eh	Device ID
0:15	RO	144Dh	Vendor ID

[Table 26] Command Register

Bits	Type	Default Value	Description
15:11	RsvdP	0h	Reserved
10	RW	0h	Interrupt Disable
9	RO	0h	Fast Back-to-Back Enable (N/A)
8	RW	0h	SERR# Enable
7	RO	0h	IDSEL Stepping/Wait Cycle Control (N/A)
6	RW	0h	Parity Error Response Enable
5	RO	0h	VGA Palette Snooping Enable (N/A)
4	RO	0h	Memory Write and Invalidate Enable (N/A)
3	RO	0h	Special Cycle Enable (N/A)
2	RW	0h	Bus Master Enable
1	RW	0h	Memory Space Enable
0	RW	0h	I/O Space Enable

[Table 27] Status Register

Bits	Type	Default Value	Description
15	RW1C	0h	Detected Parity Error
14	RW1C	0h	Signaled System Error
13	RW1C	0h	Received Master Abort
12	RW1C	0h	Received Target Abort
11	RW1C	0h	Signaled Target Abort
10:9	RO	0h	DEVSEL Timing (N/A)
8	RW1C	0h	Master Data Parity Error Detected
7	RO	0h	Fast Back-to-Back Transaction Capable (N/A)
6	RsvdZ	0h	Reserved
5	RO	0h	66MHz Capable (N/A)
4	RO	1h	Capabilities List
3	RO	0h	Interrupt Status
2:1	RsvdZ	0h	Reserved
0	RO	1h	Immediate Readiness Value

[Table 28] Revision ID Register

Bits	Type	Default Value	Description
7:0	RO	0h	Controller Hardware Revision ID

[Table 29] Class Code Register

Bits	Type	Default Value	Description
23:16	RO	1h	Base Class Code
15:8	RO	8h	Sub Class Code
7:0	RO	2h	Programming Interface

[Table 30] Cache Line Size Register

Bits	Type	Default Value	Description
7:0	RW	0h	Cache Line Size (N/A)

[Table 31] Master Latency Timer Register

Bits	Type	Default Value	Description
7:0	RO	0h	Master Latency Timer (N/A)

[Table 32] Header Type Register

Bits	Type	Default Value	Description
7	RO	0h	Multi-Function Device
6:0	RO	0h	Header Layout

[Table 33] Built In Self Test Register

Bits	Type	Default Value	Description
7	HwInit	0h	Built In Self Test (N/A)
6	RW/RO	0h	Start BIST (N/A)
5:4	RsvdP	0h	Reserved
3:0	RO	0h	Completion Code (N/A)

[Table 34] Memory Register Base Address Lower 32-bits (BAR0) Register

Bits	Type	Default Value	Description
31:15	RW	0h	Base Address
14:4	RO	0h	Reserved
3	RO	0h	Pre-Fetchable
2:1	RO	2h	Address Type (64-bit)
0	RO	0h	Memory Space Indicator (MEMSI)

[Table 35] Memory Register Base Address Upper 32-bits (BAR1)

Bits	Type	Default Value	Description
31:0	RO	0h	Base Address

[Table 36] Index/Data Pair Register Base Address (BAR2) Register

Bits	Type	Default Value	Description
31:0	RO	0h	N/A

[Table 37] BAR3 Register

Bits	Type	Default Value	Description
31:0	RO	0h	N/A

[Table 38] Vendor Specific BAR4 Register

Bits	Type	Default Value	Description
31:0	RO	0h	N/A

[Table 39] Vendor Specific BAR5 Register

Bits	Type	Default Value	Description
31:0	RO	0h	N/A

[Table 40] Cardbus CIS Pointer Register

Bits	Type	Default Value	Description
31:0	RO	0h	N/A

[Table 41] Subsystem Identifier Register

Bits	Type	Default Value	Description
31:16	RO	960GB: AA99h 1.92TB: AA9Ah 3.84TB: AA9Bh 7.68TB: AA9Ch 15.36TB: AA9Dh	Subsystem ID
15:0	RO	144Dh	Subsystem Vendor ID

[Table 42] Expansion ROM Register

Bits	Type	Default Value	Description
31:17	RW	0h	Expansion ROM Base Address
16:8	RO	0h	Reserved
7:4	RW	0h	Expansion ROM Validation Details
3:1	RW	0h	Expansion ROM Validation Status
0	RW	0h	Expansion ROM Enable/Disable

[Table 43] Capabilities Pointer Register

Bits	Type	Default Value	Description
7:0	RO	40h	Capability Pointer (Points to PCI Power Management Capability Offset)

[Table 44] Interrupt Information Register

Bits	Type	Default Value	Description
15:8	RO	01h	Interrupt Pin
7:0	RW	FFh	Interrupt Line

[Table 45] Minimum Grant Register

Bits	Type	Default Value	Description
7:0	RO	0h	Minimum Grant (N/A)

[Table 46] Maximum Latency Register

Bits	Type	Default Value	Description
7:0	RO	0h	Maximum Latency (N/A)

5.1.3 PCI Power Management Registers

[Table 47] PCI Power Management Capability Register Summary

Start Address	End Address	Symbol	Description
40h	40h	PCIPM_ID	PCI Power Management Capability ID
41h	41h	NEXTCAP	Next Capability Pointer
42h	43h	PCIPM_CAP	PC Power Management Capabilities
44h	45h	PCIPM_CS	PCI Power Management Control and Status
46h	46h	PCIPM_CSR_BSE	PMCSR_BSE Bridge Extensions
47h	47h	PCIEPM_DATA	Data

[Table 48] PCI Power Management Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	50h	Next Capability
7:0	RO	1h	Capability ID

[Table 49] PCI Power Management Capability Register

Bits	Type	Default Value	Description
15:11	RO	0h	PME Support
10	RO	0h	D2 Support
9	RO	0h	D1 Support
8:6	RO	0h	AUX Current
5	RO	0h	Device Specific Initialization
4	RO	1h	Immediate Readiness on Return to D0
3	RO	0h	PME Clock (N/A)
2:0	RO	3h	Version (Support for PCIe® Power Management Interface Spec revision 1.2)

[Table 50] PCI Power Management Control and Status Register

Bits	Type	Default Value	Description
31:24	RO	0h	Data register (N/A)
23	RO	0h	Bus Power/Clock Enable (N/A)
22	RO	0h	B2 , B3 support (N/A)
21:16	RsvdP	0h	Reserved
15	RW1CS	0h	PME_Status
14:13	RO	0h	Data Scale (N/A)
12:9	RO	0h	Data Select (N/A)
8	RW1CS	0h	PME enable
7:4	RsvdP	0h	Reserved
3	RO	1h	No Soft Reset
2	RsvdP	0h	Reserved
1:0	RW	0h	Power State

5.1.4 Message Signaled Interrupt Registers

[Table 51] Message Signaled Interrupt Capability Register Summary

Start Address	End Address	Symbol	Description
50h	51h	MSI_ID	Message Signaled Interrupt Capability ID
52h	53h	MSI_MC	Message Signaled Interrupt Message Control
54h	57h	MSI_MA	Message Signaled Interrupt Message Address
58h	5Bh	MSI_MUA	Message Signaled Interrupt Upper Address
5Ch	5Dh	MSI_MDATA	Message Signaled Interrupt Message Data
60h	63h	MSI_MMASK	Message Signaled Interrupt Mask Bits
64h	67h	MSI_MPEND	Message Signaled Interrupt Pending Bits

[Table 52] Message Signaled Interrupt Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	70h	Next Capability
7:0	RO	05h	Capability ID

[Table 53] Message Signaled Interrupt Control Register

Bits	Type	Default Value	Description
15:11	RsvdP	0h	Reserved
10	RW	0h	Extended Message Data Enable
9	RO	1h	Extended Message Data Capable
8	RO	0h	Per Vector Masking Capable
7	RO	1h	64-bit Address Capable
6:4	RW	0h	Multiple Message Enable
3:1	RO	5h	Multiple Message Capable
0	RW	0h	MSI Enable

[Table 54] Message Signaled Interrupt Lower Address Register

Bits	Type	Default Value	Description
31:2	RW	0h	Message Address
1:0	RsvdP	0h	Reserved

[Table 55] Message Signaled Interrupt Upper Address Register

Bits	Type	Default Value	Description
31:0	RW	0h	Message Upper Address

[Table 56] Message Signaled Interrupt Message Data Register

Bits	Type	Default Value	Description
31:16	RW	0h	Extended Message Data
0:15	RW	0h	Data

[Table 57] Message Signaled Interrupt Mask Bits Register

Bits	Type	Default Value	Description
31:0	RW	0h	Mask Bits

[Table 58] Message Signaled Interrupt Pending Bits Register

Bits	Type	Default Value	Description
31:0	RO	0h	Pending Bits

5.1.5 PCI Express® Capability Registers

[Table 59] PCI Express® Capability Register Summary

Start Address	End Address	Symbol	Description
70h	71h	PCIE_ID	PCI Express® Capability ID
72h	73h	PCIE_CAP	PCI Express® Capabilities
74h	77h	PCIE_DCAP	PCI Express® Device Capabilities
78h	79h	PCIE_DC	PCI Express® Device Control
7Ah	7Bh	PCIE_DS	PCI Express® Device Status
7Ch	7Fh	PCIE_LCAP	PCI Express® Link Capabilities
80h	81h	PCIE_LC	PCI Express® Link Control
82h	83h	PCIE_LS	PCI Express® Link Status
94h	97h	PCIE_DCAP2	PCI Express® Device Capabilities 2
98h	99h	PCIE_DC2	PCI Express® Device Control 2
9Ah	9Bh	PCIE_DS2	PCI Express® Device Status 2
9Ch	9Fh	PCIE_LCAP2	PCI Express® Link Capabilities 2
A0h	A1h	PCIE_LC2	PCI Express® Link Control 2
A2h	A3h	PCIE_LS2	PCI Express® Link Status 2

[Table 60] PCI Express® Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	B0h	Next Pointer (MSI-X Capability)
7:0	RO	10h	Capability ID

[Table 61] PCI Express® Capabilities Register

Bits	Type	Default Value	Description
15	RsvdP	0h	Reserved
14	RO	0h	Reserved
13:9	RO	0h	Interrupt Message Number
8	HwInit	0h	Slot Implementation (N/A)
7:4	RO	0h	Device/Port Type
3:0	RO	2h	Capability Version

[Table 62] PCI Express® Device Capabilities Register

Bits	Type	Default Value	Description
31:29	RsvdP	0h	Reserved
28	RO	1h	Function Level Reset Capability
27:26	RO	0h	Captured Slot Power Limit Scale
25:18	RO	0h	Captured Slot Power Limit Value
17	RsvdP	0h	Reserved
16	RO	0h	ERR_COR Subclass Capable
15	RO	1h	Role-based Error Reporting
14:12	RO	0h	Reserved
11:9	RO	7h	Endpoint L1 Acceptable Latency
8:6	RO	7h	Endpoint L0 Acceptable Latency
5	RO	1h	Extended Tag Field Supported
4:3	RO	0h	Phantom Functions Supported
2:0	RO	2h	Max Payload Size Supported (512 byte payload)

[Table 63] PCI Express® Device Control Register

Bits	Type	Default Value	Description
15	RO	0h	Initiate Function Level Reset
14:12	RW	2h	Max Read Request Size
11	RW	1h	Enable No Snoop
10	RWS	0h	Aux Power PM Enable (N/A)
9	RW	0h	Phantom Functions Enable (N/A)
8	RW	1h	Extended Tag Enable
7:5	RW	0h	Max Payload Size
4	RW	1h	Enable Relaxed Ordering
3	RW	0h	Unsupported Request Reporting Enable
2	RW	0h	Fatal Error Reporting Enablehf
1	RW	0h	Non-Fatal Error Reporting Enable
0	RW	0h	Correctable Error Reporting Enable

[Table 64] PCI Express® Device Status Register

Bits	Type	Default Value	Description
15:7	RsvdZ	0h	Reserved
6	RO	0h	Emergency Power Reduction Detected (N/A)
5	RO	0h	Transactions Pending
4	RW	0h	Aux Power Detected
3	RW1C	0h	Unsupported Request Detected
2	RW1C	0h	Fatal Error Detected
1	RW1C	0h	Non-Fatal Error Detected
0	RW1C	0h	Correctable Error Detected

[Table 65] PCI Express® Link Capabilities Register

Bits	Type	Default Value	Description
31:24	HwInit	0h (Port 0)	Port Number
23	RsvdP	0h	Reserved
22	HwInit	1h	ASPM Optionality Compliance
21	RO	0h	Link Bandwidth Notification Capability
20	RO	0h	Data Link Layer Link Active Reporting Capable
19	RO	0h	Surprise Down Error Reporting Capable
18	RO	0h	Clock Power Management
17:15	RO	6h	L1 Exit Latency
14:12	RO	7h	L0s Exit Latency
11:10	RO	0h	Active State Power Management Support
9:4	RO	4h (x4 link)	Maximum Link Width
3:0	RO	5h	Supported Link Speeds

[Table 66] PCI Express® Link Control Register

Bits	Type	Default Value	Description
15:14	RW/RsvdP	0h	DRS Signaling Control (N/A)
13:12	RsvdP	0h	Reserved
11	RsvdP	0h	Link Autonomous Bandwidth Interrupt Enable (N/A)
10	RsvdP	0h	Link Bandwidth Management Interrupt Enable (N/A)
9	RsvdP	0h	Hardware Autonomous Width Disable
8	RW	0h	Enable Clock Power Management
7	RW	0h	Extended Sync
6	RW	0h	Common Clock Configuration
5	RsvdP	0h	Retrain Link (N/A)
4	RsvdP	0h	Link Disable (N/A)
3	RW	0h	Read Completion Boundary
2	RsvdP	0h	Reserved
1:0	RW	0h	Active State Power Management Control

[Table 67] PCI Express® Link Status Register

Bits	Type	Default Value	Description
15	RO	0h	Link Autonomous Bandwidth Status (N/A)
14	RO	0h	Link Bandwidth Management Status (N/A)
13	RO	0h	Data Link Layer Link Active
12	HwInit	1h	Slot Clock Configuration
11	RO	0h	Link Training (N/A)
10	RO	0h	Reserved
9:4	RO	1h	Negotiated Link Width
3:0	RO	1h	Current Link Speed

[Table 68] PCI Express® Device Capabilities 2 Register

Bits	Type	Default Value	Description
31	HwInit	0h	FRS Supported
30:27	RsvdP	0h	Reserved
26	RO	0h	Emergency Power Reduction Initialization Required (N/A)
25:24	RO	0h	Emergency Power Reduction Supported (N/A)
23:22	HwInit	1h	Max End-End TLP Prefixes
21	HwInit	1h	End-End TLP Prefix Supported
20	RO	1h	Extended Format Field Supported
19:18	HwInit	0h	OBFF Supported
17	HwInit	0h	10-Bit Tag Requester Supported
16	HwInit	1h	10-Bit Tag Completer Supported
15:14	HwInit	0h	LN System CLS (N/A)
13:12	RO	0h	TPH Completer Supported
11	RO	1h	Latency Tolerance Reporting Supported
10	HwInit	0h	No RO-enabled PR-PR Passing (N/A)
9	RO	0h	128-bit CAS Completer Supported
8	RO	0h	64-bit Atomic Op Com pleter Supported
7	RO	0h	32-bit Atomic Op Completer Supported
6	RO	0h	Atomic Op Routing Supported (N/A)
5	RO	0h	ARI Forwarding Supported (N/A)
4	RO	1h	Completion Timeout Disable Supported
3:0	HwInit	Fh	Completion Timeout Ranges Supported

[Table 69] PCI Express® Device Control 2 Register

Bits	Type	Default Value	Description
15	RsvdP	0h	End-to-end TLP Prefix Blocking (N/A)
14:13	RW/RsvdP	0h	OBFF Enable (N/A)
12	RW	0h	10-Bit Tag Requester Enable (N/A)
11	RO	0h	Emergency Power Reduction Request (N/A)
10	RW/RsvdP	0h	Latency Tolerance Reporting Mechanism Enable
9	RW	0h	IDO Completion Enable (N/A)
8	RW	0h	IDO Request Enable (N/A)
7	RW	0h	AtomicOp Egress Blocking (N/A)
6	RW	0h	AtomicOp Requester Enable (N/A)
5	RW	0h	ARI Forwarding Enable (N/A)
4	RW	0h	Completion Timeout Disable
3:0	RW	0h	Completion Timeout Value

[Table 70] PCI Express® Device Status 2 Register

Bits	Type	Default Value	Description
15:0	RsvdZ	0h	Reserved

[Table 71] PCI Express® Link Capabilities 2 Register

Bits	Type	Default Value	Description
31	RO	1h	DRS supported
30:25	RsvdP	0h	Reserved
24	HWinit	1h	Two Retimers Presence Detect Supported
23	HWinit	1h	Retimer Presence Detect Supported
22:16	RO	0h	Lower SKP OS Reception Supported Speed Vector (N/A)
15:9	RO	0h	Lower SKP OS Generation Supported Speed Vector (N/A)
8	RO	0h	Cross-Link Supported
7:1	RO	1Fh	Supported Speeds Vector
0	RsvdP	0	Reserved

[Table 72] PCI Express® Link Control 2 Register

Bits	Type	Default Value	Description
15:12	RWS/RsvdP	0h	Compliance De-emphasis
11	RWS/RsvdP	0h	Compliance SOS
10	RWS/RsvdP	0h	Enter Modified Compliance
9:7	RWS/RsvdP	0h	Transmit Margin
6	HwInit	0h	Selectable De-Emphasis (N/A)
5	RWS/RsvdP	0h	Hardware Autonomous Speed Disable
4	RWS/RsvdP	0h	Enter Compliance
3:0	RWS/RsvdP	5h	Target Link Speed 1h: 2.5 GT/s (Gen.1) 2h: 5.0 GT/s (Gen.2) 3h: 8.0 GT/s (Gen. 3) 4h: 16 GT/s (Gen. 4) 5h: 32 GT/s (Gen. 5)

[Table 73] PCI Express® Link Status 2 Register

Bits	Type	Default Value	Description
15	RO	0h	DRS Message Received (N/A)
14:12	RO	0h	Downstream Componenet Present (N/A)
11:10	RsvdZ	0h	Reserved
9:8	RO	1h	Crosslink Resolution
7	ROS/RsvdZ	0h	Two Retimers Presence Detected
6	ROS/RsvdZ	0h	Retimer Presence Detected
5	RW1CS	0h	Link Equalization Request
4	ROS	0h	Equalization Phase 3 Successful
3	ROS	0h	Equalization Phase 2 Successful
2	ROS	0h	Equalization Phase 1 Successful
1	ROS	0h	Equalization Complete
0	RO	1h	Current De-Emphasis

5.1.6 MSI-X Registers

[Table 74] MSI-X Capability Register Summary

Start Address	End Address	Symbol	Description
B0h	B1h	MSIX_ID	MSI-X Capability ID
B2h	B3h	MSIX_CAP	MSI-X Message Control
B4h	B7h	MSIX_TBL	MSI-X Table Offset and Table BIR
B8h	BBh	MSIX_PBA	MSI-X PBA Offset and PBA BIR

[Table 75] MSI-X Identifier Register

Bits	Type	Default Value	Description
15:8	RO	00h	Next Capability
7:0	RO	11h	Capability ID

[Table 76] MSI-X Control Register

Bits	Type	Default Value	Description
15	RW	0h	MSI-X Enable
14	RW	0h	Function Mask
13:11	RsvdP	0h	Reserved
10:0	RO	102h	Table Size

[Table 77] MSI-X Table Offset Register

Bits	Type	Default Value	Description
31:3	RO	600h	Table Offset
2:0	RO	0h	Table BIR

[Table 78] MSI-X Pending Bit Array Offset Register

Bits	Type	Default Value	Description
31:3	RO	400h	Pending Bit Array Offset
2:0	RO	0h	Pending Bit Array BIR

5.1.7 Advanced Error Reporting Registers

[Table 79] Advanced Error Reporting Capability Register Summary

Start Address	End Address	Symbol	Description
100h	103h	AER_ID	AER Capability ID
104h	107h	AER_UCES	AER Uncorrectable Error Status
108h	10Bh	AER_UCEM	AER Uncorrectable Error Mask
10Ch	10Fh	AER_UCESEV	AER Uncorrectable Error Severity
110h	113h	AER_CES	AER Correctable Error Status
114h	117h	AER_CEM	AER Correctable Error Mask
118h	11Bh	AER_CC	AER Advanced Error Capabilities and Control
11Ch	12Bh	AER_HL	AER Header Log

[Table 80] AER Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	168h	Next Pointer (Points to Alternative Routing-ID Capability Header Offset)
19:16	RO	2h	Capability Version
15:0	RO	1h	Capability ID

[Table 81] AER Uncorrectable Error Status Register

Bits	Type	Default Value	Description
31	RsvdZ	0h	Reserved
30	RW1CS	0h	PCRC Check Failed Status
29	RW1CS	0h	Misrouted IDE TLP Status
28	RW1CS	0h	IDE Check Failed Status
27	RsvdZ	0h	Reserved
26	RW1CS	0h	Poisoned TLP Egress Blocked Status (N/A)
25	RW1CS	0h	TLP Prefix Blocked Error Status
24	RW1CS	0h	Atomic Op Egress Blocked Status (N/A)
23	RW1CS	0h	MC Blocked TLP Status (N/A)
22	RW1CS	0h	Uncorrectable Internal Error Status
21	RW1CS	0h	ACS Violation Status (N/A)
20	RW1CS	0h	Unsupported Request Error Status
19	RW1CS	0h	ECRC Error Status
18	RW1CS	0h	Malformed TLP Status
17	RW1CS	0h	Receiver Overflow Status
16	RW1CS	0h	Unexpected Completion Status
15	RW1CS	0h	Completer Abort Status
14	RW1CS	0h	Completion Timeout Status
13	RW1CS	0h	Flow Control Protocol Error Status
12	RW1CS	0h	Poisoned TLP Status
11:6	RsvdZ	0h	Reserved
5	RW1CS	0h	Surprise Down Error Status (N/A)
4	RW1CS	0h	Data Link Protocol Error Status
3:1	RsvdZ	0h	Reserved
0	Undefined	0h	Undefined

[Table 82] AER Uncorrectable Error Mask Register

Bits	Type	Default Value	Description
31	RsvdZ	0h	Reserved
30	RW1CS	0h	PCRC Check Failed Mask
29	RW1CS	0h	Misrouted IDE TLP Mask
28	RW1CS	0h	IDE Check Failed Mask
27	RsvdZ	0h	Reserved
26	RWS	0h	Poisoned TLP Egress Blocked Mask
25	RWS	0h	TLP Prefix Blocked Error Mask
24	RWS	0h	Atomic Op Egress Blocked Mask
23	RWS	0h	MC Blocked TLP Mask
22	RWS	1h	Uncorrectable Internal Error Mask
21	RWS	0h	ACS Violation Mask
20	RWS	0h	Unsupported Request Error Mask
19	RWS	0h	ECRC Error Mask
18	RWS	0h	Malformed TLP Mask
17	RWS	0h	Receiver Overflow Mask
16	RWS	0h	Unexpected Completion Mask
15	RWS	0h	Completer Abort Mask
14	RWS	0h	Completion Timeout Mask
13	RWS	0h	Flow Control Protocol Error Mask
12	RWS	0h	Poisoned TLP Mask
11:6	RsvdZ	0h	Reserved
5	RWS	0h	Surprise Down Error Mask (N/A)
4	RWS	0h	Data Link Protocol Error Mask
3:1	RsvdZ	0h	Reserved
0	Undefined	0h	Undefined

[Table 83] AER Uncorrectable Error Severity Register

Bits	Type	Default Value	Description
31	RsvdP	0h	Reserved
30	RW1CS	0h	PCRC Check Failed Severity
29	RW1CS	0h	Misrouted IDE TLP Severity
28	RW1CS	1h	IDE Check Failed Severity
27	RsvdZ	0h	Reserved
26	RWS	0h	Poisoned TLP Egress Blocked Severity
25	RWS	0h	TLP Prefix Blocked Error Severity
24	RWS	0h	Atomic Op Egress Blocked Severity
23	RWS	0h	MC Blocked TLP Severity
22	RWS	1h	Uncorrectable Internal Error Severity
21	RWS	0h	ACS Violation Severity
20	RWS	0h	Unsupported Request Error Severity
19	RWS	0h	ECRC Error Severity
18	RWS	1h	Malformed TLP Severity
17	RWS	1h	Receiver Overflow Severity
16	RWS	0h	Unexpected Completion Severity
15	RWS	0h	Completer Abort Severity
14	RWS	0h	Completion Timeout Severity
13	RWS	1h	Flow Control Protocol Error Severity
12	RWS	0h	Poisoned TLP Severity
11:6	RsvdP	0h	Reserved
5	RWS	1h	Surprise Down Error Severity (N/A)
4	RWS	1h	Data Link Protocol Error Severity
3:1	RsvdP	0h	Reserved
0	Undefined	0h	Undefined

[Table 84] AER Correctable Error Status Register

Bits	Type	Default Value	Description
31:16	RsvdZ	0h	Reserved
15	RW1CS	0h	Header Log Overflow Status
14	RW1CS	0h	Corrected Internal Error Status
13	RW1CS	0h	Advisory Non-Fatal Error Status
12	RW1CS	0h	Replay Timer Timeout Status
11:9	RsvdZ	0h	Reserved
8	RW1CS	0h	Replay Number Rollover Status
7	RW1CS	0h	Bad DLLP Status
6	RW1CS	0h	Bad TLP Status
5:1	RsvdZ	0h	Reserved
0	RW1CS	0h	Received Error Status

[Table 85] AER Correctable Error Mask Register

Bits	Type	Default Value	Description
31:16	RsvdP	0h	Reserved
15	RWS	1h	Header Log Overflow Mask
14	RWS	1h	Corrected Internal Error Mask
13	RWS	1h	Advisory Non-Fatal Error Mask
12	RWS	0h	Replay Timer Timeout Mask
11:9	RsvdP	0h	Reserved
8	RWS	0h	Replay Number Rollover Mask
7	RWS	0h	Bad DLLP Mask
6	RWS	0h	Bad TLP Mask
5:1	RsvdP	0h	Reserved
0	RWS	0h	Received Error Mask

[Table 86] AER Capabilities and Control Register

Bits	Type	Default Value	Description
31:13	RsvdP	0h	Reserved
12	RO	0h	Completion Timeout Prefix/Header Log Capable
11	ROS	0h	TLP Prefix Log Present
10	RWS	0h	Multiple Header Recording Enable
9	RO	1h	Multiple Header Recording Capable
8	RWS	0h	ECRC Check Enable
7	RO	1h	ECRC Check Capable
6	RWS	0h	ECRC Generation Enable
5	RO	1h	ECRC Generation Capable
4:0	ROS	0h	First Error Pointer

[Table 87] AER Header Log Register

Bits	Type	Default Value	Description
127:120	ROS	0h	Header Byte 0
119:112	ROS	0h	Header Byte 1
111:104	ROS	0h	Header Byte 2
103:96	ROS	0h	Header Byte 3
95:88	ROS	0h	Header Byte 4
87:80	ROS	0h	Header Byte 5
79:72	ROS	0h	Header Byte 6
71:64	ROS	0h	Header Byte 7
63:56	ROS	0h	Header Byte 8
55:48	ROS	0h	Header Byte 9
47:40	ROS	0h	Header Byte 10
39:32	ROS	0h	Header Byte 11
31:24	ROS	0h	Header Byte 12
23:16	ROS	0h	Header Byte 13
15:8	ROS	0h	Header Byte 14
7:0	ROS	0h	Header Byte 15

5.1.8 Secondary PCI Express® Capability Registers

[Table 88] Secondary PCI Express® Capability Register Summary

Start Address	End Address	Symbol	Description
168h	16Bh	SPE_ID	Secondary PCI Express® Capability
16Ch	16Fh	PCIE_LC3	PCI Express® Link Control 3
170h	173h	PCIE_LE	PCI Express® Lane Error Status
174h	175h	PCIE_L0EC	PCI Express® Lane 0 Equalization Control
176h	177h	PCIE_L1EC	PCI Express® Lane 1 Equalization Control
178h	179h	PCIE_L2EC	PCI Express® Lane 2 Equalization Control
17Ah	17Bh	PCIE_L3EC	PCI Express® Lane 3 Equalization Control

[Table 89] Secondary PCI Express® Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	188h	Next Pointer
19:16	RO	1h	Capability Version
15:0	RO	19h	Capability ID (Secondary PCI Express® Extended capability)

[Table 90] PCI Express® Link Control 3 Register

Bits	Type	Default Value	Description
31:16	Rsvdp	0h	Reserved
15:9	RW	0h	Enable Lower SKP OS Generation Vector
8:2	RsvdP	0h	Reserved
1	RW	0h	Link Equalization Request Interrupt Enable
0	RW	0h	Perform Equalization (N/A)

[Table 91] PCI Express® Lane Error Status Register

Bits	Type	Default Value	Description
31:4	Rsvdp	0h	Reserved
3:0	RW1CS	0h	Lane Error Status Bits

[Table 92] PCI Express® Lane 0 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0h	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RsvdP	0h	Reserved
6:4	HwInit/RsvdP	0h	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0h	Downstream Port 8.0T/s Transmitter Preset (N/A)

[Table 93] PCI Express® Lane 1 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0h	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RsvdP	0h	Reserved
6:4	HwInit/RsvdP	0h	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0h	Downstream Port 8.0T/s Transmitter Preset (N/A)

[Table 94] PCI Express® Lane 2 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0h	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RsvdP	0h	Reserved
6:4	HwInit/RsvdP	0h	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0h	Downstream Port 8.0T/s Transmitter Preset (N/A)

[Table 95] PCI Express® Lane 3 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0h	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RsvdP	0h	Reserved
6:4	HwInit/RsvdP	0h	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0h	Downstream Port 8.0T/s Transmitter Preset (N/A)

5.1.9 Physical Layer 16.0 GT/s Capability register

[Table 96] Physical Layer 16.0 GT/s Capability Summary

Start Address	End Address	Symbol	Description
188h	18Bh		Physical Layer 16.0 GT/s Extended Capability Header
18Ch	18Fh		16.0 GT/s Capabilities Register
190h	193h		16.0 GT/s Control Register
194h	197h		16.0 GT/s Status Register
198h	19Bh		16.0 GT/s Local Data Parity Mismatch Status Register
19Ch	19Fh		16.0 GT/s First Retimer Data Parity Mismatch Status Register
1A0h	1A3h		16.0 GT/s Second Retimer Data Parity Mismatch Status Register
1A4h	1A7h		Reserved
1A8h	1ABh		16.0 GT/s Control Register for Lane 0-3

[Table 97] Physical Layer 16.0 GT/s Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	1ACh	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	26h	Capability ID (Secondary PCI Express® Extended capability)

[Table 98] 16.0 GT/s Capabilities Register

Bits	Type	Default Value	Description
31:0	RsvdP	0	Reserved

[Table 99] 16.0 GT/s Control Register

Bits	Type	Default Value	Description
31:0	RsvdP	0	Reserved

[Table 100] 16.0 GT/s Status Register

Bits	Type	Default Value	Description
31:5	RsvdZ	0	Reserved
4	RW1CS	0	Link Equalization Request 16.0 GT/s
3	ROS	0	Equalization 16.0 GT/s Phase 3 Successful
2	ROS	0	Equalization 16.0 GT/s Phase 2 Successful
1	ROS	0	Equalization 16.0 GT/s Phase 1 Successful
0	ROS	0	Equalization 16.0 GT/s Complete

[Table 101] 16.0 GT/s Local Data Parity Mismatch Status Register

Bits	Type	Default Value	Description
31:4	RsvdP	0	Reserved
3:0	RW1CS	0	Local Data Parity Mismatch Status

[Table 102] 16.0 GT/s First Retimer Data Parity Mismatch Status Register

Bits	Type	Default Value	Description
31:4	RsvdP	0	Reserved
3:0	RW1CS	0	First Retimer Data Parity Mismatch Status

[Table 103] 16.0 GT/s Second Retimer Data Parity Mismatch Status Register

Bits	Type	Default Value	Description
31:4	RsvdP	0	Reserved
3:0	RW1CS	0	Second Retimer Data Parity Mismatch Status

[Table 104] Reserved

Bits	Type	Default Value	Description
31:0	RsvdP	0	Reserved

[Table 105] 16.0 GT/s Control Register for Lane 0-3

Bits	Type	Default Value	Description
31:28	HwInit/RO	Fh	Upstream Port 16.0 GT/s Transmitter Preset Lane 3
27:24	HwInit/RsvdP	0h	Downstream Port 16.0 GT/s Transmitter Preset Lane 3 (N/A)
23:20	HwInit/RO	Fh	Upstream Port 16.0 GT/s Transmitter Preset Lane 2
19:16	HwInit/RsvdP	0h	Downstream Port 16.0 GT/s Transmitter Preset Lane 2 (N/A)
15:12	HwInit/RO	Fh	Upstream Port 16.0 GT/s Transmitter Preset Lane 1
11:8	HwInit/RsvdP	0h	Downstream Port 16.0 GT/s Transmitter Preset Lane 1 (N/A)
7:4	HwInit/RO	Fh	Upstream Port 16.0 GT/s Transmitter Preset Lane 0
3:0	HwInit/RsvdP	0h	Downstream Port 16.0 GT/s Transmitter Preset Lane 0 (N/A)

5.1.10 Margining Extended Capability Header register

[Table 106] Margining Extended Capability Header Summary

Start Address	End Address	Symbol	Description
1ACh	1AFh		Margining Extended Capability Header
1B0h	1B1h		Margining Port Capabilities Register
1B2h	1B3h		Margining Port Status Register
1B4h	1B5h		Margining Lane Control Register (Lane 0)
1B6h	1B7h		Margining Lane Status Register (Lane 0)
1B8h	1B9h		Margining Lane Control Register (Lane 1)
1BAh	1BBh		Margining Lane Status Register (Lane 1)
1BCh	1BDh		Margining Lane Control Register (Lane 2)
1BEh	1BFh		Margining Lane Status Register (Lane 2)
1C0h	1C1h		Margining Lane Control Register (Lane 3)
1C2h	1C3h		Margining Lane Status Register (Lane 3)

[Table 107] Margining Extended Capability Header Register

Bits	Type	Default Value	Description
31:20	RO	364h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	27h	PCI Express® Extended Capability ID

[Table 108] Margining Port Capabilities Register

Bits	Type	Default Value	Description
15:1	RsvdP	0	Reserved
0	HWInit	0	Margining uses Driver Software

[Table 109] Margining Port Status Register

Bits	Type	Default Value	Description
15:2	RsvdP	0	Reserved
1	RO	0	Margining Software Ready
0	RO	0	Margining Ready

[Table 110] Margining Lane Control Register Lane 0

Bits	Type	Default Value	Description
15:8	RW	9Ch	Margin Payload
7	RsvdP	0	Reserved
6	RW	0	Usage Model
5:3	RW	7h	Margin Type
2:0	RW	0	Receiver Number

[Table 111] Margining Lane Status Register Lane 0

Bits	Type	Default Value	Description
15:8	RW	0	MarginPayload Status
7	RsvdP	0	Reserved
6	RW	0	Usage Model Status
5:3	RW	0	Margin Type Status
2:0	RW	0	Receiver Number Status

[Table 112] Margining Lane Control Register Lane 1

Bits	Type	Default Value	Description
15:8	RW	9Ch	Margin Payload
7	RsvdP	0	Reserved
6	RW	0	Usage Model
5:3	RW	7h	Margin Type
2:0	RW	0	Receiver Number

[Table 113] Margining Lane Status Register Lane 1

Bits	Type	Default Value	Description
15:8	RW	0	MarginPayload Status
7	RsvdP	0	Reserved
6	RW	0	Usage Model Status
5:3	RW	0	Margin Type Status
2:0	RW	0	Receiver Number Status

[Table 114] Margining Lane Control Register Lane 2

Bits	Type	Default Value	Description
15:8	RW	9Ch	Margin Payload
7	RsvdP	0	Reserved
6	RW	0	Usage Model
5:3	RW	7h	Margin Type
2:0	RW	0	Receiver Number

[Table 115] Margining Lane Status Register Lane 2

Bits	Type	Default Value	Description
15:8	RW	0	MarginPayload Status
7	RsvdP	0	Reserved
6	RW	0	Usage Model Status
5:3	RW	0	Margin Type Status
2:0	RW	0	Receiver Number Status

[Table 116] Margining Lane Control Register Lane 3

Bits	Type	Default Value	Description
15:8	RW	9Ch	Margin Payload
7	RsvdP	0	Reserved
6	RW	0	Usage Model
5:3	RW	7h	Margin Type
2:0	RW	0	Receiver Number

[Table 117] Margining Lane Status Register Lane 3

Bits	Type	Default Value	Description
15:8	RW	0	MarginPayload Status
7	RsvdP	0	Reserved
6	RW	0	Usage Model Status
5:3	RW	0	Margin Type Status
2:0	RW	0	Receiver Number Status

5.1.11 Data Link Feature Extended Capability register

[Table 118] Data Link Feature Extended Summary

Start Address	End Address	Symbol	Description
364h	367h		Data Link Feature Extended Capability Header
368h	36Bh		Data Link Feature Capabilities Register
36Ch	36Fh		Data Link Feature Status Register

[Table 119] Data Link Feature Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	000h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	25h	PCI Express Extended Capability ID

[Table 120] Data Link Feature Capabilities Register

Bits	Type	Default Value	Description
31	HwInit	1h	Data Link Feature Exchange Enable
30:23	RsvdP	0h	Reserved
22:1	RsvdP	0h	Reserved
0	HwInit	1h	Local Scaled Flow Control Supported

[Table 121] Data Link Feature Status Register

Bits	Type	Default Value	Description
31	RO	0h	Remote Data Link Feature Supported Valid
30:23	RsvdP	0h	Reserved
22:1	RO	0h	Undefined
0	RO	0h	Remote Scaled Flow Control Supported

5.2 NVM Express™ Registers

5.2.1 Register Summary

[Table 122] Register Summary

Start Address	End Address	Name	Type
00h	07h	CAP	Controller Capabilities
08h	0Bh	VS	Version
0Ch	0Fh	INTMS	Interrupt Mask Set
10h	13h	INTMC	Interrupt Mask Clear
14h	17h	CC	Controller Configuration
18h	1Bh	Reserved	Reserved
1Ch	1Fh	CSTS	Controller Status
20h	23h	NSSR	NVM Subsystem Reset
24h	27h	AQA	Admin Queue Attributes
28h	2Fh	ASQ	Admin Submission Queue Base Address
30h	37h	ACQ	Admin Completion Queue Base Address
38h	EFFh	Reserved	Reserved
F00h	FFFh	Reserved	Command Set Specific
1000h	1003h	SQ0TDBL	Submission Queue 0 Tail Doorbell (Admin)
1000h + (1 * (4 << CAP.DSTRD))	1003h + (1 * (4 << CAP.DSTRD))	CQ0HDBL	Completion Queue 0 Head Doorbell (Admin)
...			
1000h+ (2y * (4 << CAP.DSTRD))	1003h + (2y * (4 << CAP.DSTRD))	SQyTDVL	Submission Queue y Tail Doorbell
1000h + ((2y + 1) * (4 << CAP.DSTRD))	1003h + ((2y + 1) * (4 << CAP.DSTRD))	CQYHDBL	Completion Queue y Head Doorbell

5.2.2 Controller Registers

[Table 123] Controller Capabilities

Bits	Type	Name	Default Value	Description
63:61	RO	-	0h	Reserved
60:59	RO	CRMS	3h	bit 0: Controller Ready With Media Support (CRWMS) bit 1: Controller Ready Independent of Media Support (CRIMS)
58	RO	NSSS	0h	NVM Subsystem Shutdown Supported (NSSS)
57	RO	CMBS	0h	Controller Memory Buffer Supported (CMBS)
56	RO	PMRS	0h	Persistent Memory Region Supported (PMRS)
55:52	RO	MPSMAX	1h	Memory Page Size Maximum (Maximum is 8KB)
51:48	RO	MPSMIN	0h	Memory Page Size Minimum (Minimum is 4KB)
47:45	RO	-	0h	Reserved
44:37	RO	CSS	1h	Command Sets Supported 1h: NVM command set
36	RO	NSSRS	1h	NVM Subsystem Reset Supported
35:32	RO	DSTRD	0h	Doorbell Stride 0: Stride of 4 bytes
31:24	RO	TO	960GB: 28h 1.92TB: 28h 3.84TB: 28h 7.68TB: 3Ch 15.36TB: 50h	Timeout(unit:500ms) 28h: 20 seconds 3Ch: 30 seconds 50h: 40 seconds
23:19	RO	-	0h	Reserved
18:17	RO	AMS	1h	Arbitration Mechanism Supported (Weighted Round Robin with Urgent supported)
16	RO	CQR	1h	Contiguous Queues Required
15:0	RO	MQES	3FFFh	Maximum Queue Entries Supported (16384 entries supported)

[Table 124] Version

Bits	Type	Name	Default Value	Description
31:16	RO	MJR	2h	Major Version Number
15:0	RO	MNR	0h	Minor Version Number

NOTE: The PM9D3a supports NVM Express™ version 2.0.

[Table 125] Interrupt Mask Set

Bits	Type	Name	Default Value	Description
31:0	RW1S	IVMS	0h	Interrupt Vector Mask Set

[Table 126] Interrupt Mask Clear

Bits	Type	Name	Default Value	Description
31:00	RW1C	IVMC	0h	Interrupt Vector Mask Clear

[Table 127] Controller Configuration

Bits	Type	Name	Default Value	Description
31:24	RO	-	0h	Reserved
23:20	RW	IOCQES	0h	I/O Completion Queue Entry Size (Configured as a power of 2) (Should be set to 4 for a 16 byte entry size)
19:16	RW	IOSQES	0h	I/O Submission Queue Entry Size (Configured as a power of 2) (Should be set to 6 for a 64 byte entry size)
15:14	RW	SHN	0h	Shutdown Notification 0h: No notification 1h: Normal shutdown notification 2h: Abrupt shutdown notification 3h: Reserved CSTS.SHST indicates shutdown status.
13:11	RW	AMS	0h	Arbitration Mechanism Selected 0h: Round Robin No other values supported.
10:7	RW	MPS	0h	Memory Page Size MPS is 2^(12+MPS) Shall be within CAP.MPSMAX and CAP.MPSMIN ranges.
6:4	RW	CSS	0h	Command Set Selected 0h: NVM Command Set No other values supported
3:1	RO	-	0h	Reserved
0	RW	EN	0h	Enable When set to 1, controller shall process commands. When cleared to 0, controller shall not process commands. This field is subject to CSTS.RDY and CAP.TO restrictions.

[Table 128] Controller Status

Bits	Type	Name	Default Value	Description
31:6	RO	-	0h	Reserved
5	RW	PP	0h	Processing Paused
4	RW1C	NSSRO	0h	NVM Subsystem Reset Occurred
3:2	RO	SHST	0h	Shutdown Status 0h: Normal operation, no shutdown requested 1h: Shutdown processing occurring 2h: Shutdown processing complete 3h: Reserved
1	RO	CFS	0h	Controller Fatal Status
0	RO	RDY	0h	1h: Controller ready to process commands 0h: Controller shall not process commands.

[Table 129] NVM Subsystem Reset

Bits	Type	Name	Default Value	Description
31:0	RW	NSSRC-	0h	NVM Subsystem Reset Control

[Table 130] Admin Queue Attributes

Bits	Type	Name	Default Value	Description
31:28	RO	-	0h	Reserved
27:16	RW	ACQS	0h	Admin Completion Queue Size Max: 4096 (Value of 4095h - 0's based value)
15:12	RO	-	0h	Reserved
11:0	RW	ASQS	0h	Admin Submission Queue Size Max: 4096 (Value of 4095h - 0's based value)

[Table 131] Admin Submission Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ASQB	0h	Admin Submission Queue Base Address
11:0	RO	-	0h	Reserved

[Table 132] Admin Completion Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ACQB	0h	Admin Completion Queue Base Address
11:0	RO	-	0h	Reserved

[Table 133] Submission Queue Tail y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO	-	0h	Reserved
15:0	RW	SQT	0h	Submission Queue Tail

[Table 134] Completion Queue Head y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO	-	0h	Reserved
15:0	RW	CQH	0h	Completion Queue Head

6.0 SUPPORTED COMMAND SET

The Admin command sets and NVM I/O command sets of Samsung SSD PM9D3a are defined in compliant with NVM Express™ specification revision 2.0

6.1 Admin Command Set

The Admin command set is the commands that are submitted to the Admin Submission Queues.
The detailed specifications are described in NVM Express™ specification document.

[Table 135] Opcode for Admin Commands

Opcode (Hex)	Command Name
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Feature
0Ah	Get Feature
0Ch	Asynchronous Event Request
0Dh	Namespace Management
10h	Firmware Commit
11h	Firmware Image Download
14h	Device Self-test
15h	Namespace Attachment
18h	Keep Alive
19h	Directive Send
1Ah	Directive Receive
1Ch	Virtualization Management (Not support)
1Dh	NVMe-MI™ Send
1Eh	NVMe-MI™ Receive
7Ch	Doorbell Buffer Config (Not support)
80h - BFh	I/O Command Set Specific
C0h - FFh	Vendor Specific

6.1.1 Identify Command

The Identify Command returns the data described below.

[Table 136] Identify Controller Data Structure

Bytes	O/M	Default Value	Description
1:0	M	144Dh	PCI Vendor ID
3:2	M	144Dh	PCI Subsystem Vendor ID
23:4	M	S##############	Serial Number(ASCII), # :Variables
63:24	M	960GB: SAMSUNG MZWL6960HFJA-00B07 1.92TB: SAMSUNG MZWL61T9HFLT-00B07 3.84TB: SAMSUNG MZWL63T8HFLT-00B07 7.68TB: SAMSUNG MZWL67T6HBLC-00B07 15.36TB: SAMSUNG MZWL615THBLF-00B07	Model Number (ASCII)
71:64	M	########	Firmware Revision, #:Variables
72	M	2h	Recommended Arbitration Burst
75:73	M	002538h	IEEE OUI
76	O	0h	Multi-Interface Capabilties and Namespace Sharing Capability Bit 2: 1h - Controller is associated with an SR-IOV Virtual Function 0h - Controller is associated with a PCI Function. Bit 1: 1h - Device has Two or More controller 0h - Device has One Controller Bit 0: 1h - Device has Two or More physical PCI Express ports 0h - Device has One PCI Express port
77	M	6h	Maximum Data Transfer Size
79:78	M	7h	Controller ID (CNTLID)
83:80	M	20000h	Controller Version
87:84	M	960GB, 1.92TB, 3.84TB, 7.68TB: 7A1200h 15.36TB: B71B00h	RTD3 Resume Laterncy
91:88	M	960GB, 1.92TB, 3.84TB, 7.68TB: 7A1200h 15.36TB: 989680h	RTD3 Entry Latancy
95:92	M	2300h	Optional Asynchronous Events Supported (OAES)
99:96	M	280h	Controller Attributes (CTRATT)
101:100	O	0h	Read Recovery Levels Supported (RRLS)
110:102	-	0h	Reserved
111	M	1h	Controller Type (CNTRLTYPE)
127:112	O		FRU Globally Unique Identifier (FGUID)
239:128	-	0h	Reserved
252:240	M	-	NVMe™ Management Interface Specification for Definition
253	M	1h	NVM Subsystem Report (NVMSR)
254	M	0h	VPD Write Cycle Information (VWCI)
255	M	1h	Management Endpoint Capabilities (MEC)

257:256	M	25Fh	Optional Admin Command Support Bits 15:10 are reserved. Bit 9 if set to '1', then the controller supports the Get LBA Status capability (refer to section 8.22). If cleared to '0', then the controller does not support the Get LBA Status capability. Bit 8 if set to '1', then the controller supports the Doorbell Buffer Config command. If cleared to '0', then the controller does not support the Doorbell Buffer Config command. Bit 7 if set to '1', then the controller supports the Virtualization Management command. If cleared to '0', then the controller does not support the Virtualization Management command. Bit 6 if set to '1', then the controller supports the NVMe-MI™ Send and NVMe-MI™ Receive commands. If cleared to '0', then the controller does not support the NVMe-MI™ Send and NVMe-MI™ Receive commands. Bit 5 if set to '1' then the controller supports Directives. If cleared to '0' then the controller does not support Directives. A controller that supports Directives shall support the Directive Send and Directive Receive commands. Refer to section 9. Bit 4 if set to '1' then the controller supports the Device Self-test command. If cleared to '0' then the controller does not support the Device Self-test command. Bit 3: 1h - Namespace Management and Namespace Attachment Commands Supported Bit 2: 1h – Firmware Activate/Download Supported Bit 1: 1h Format NVM Supported Bit 0: 0 Security Send and Security Receive Not Supported
258	M	7h	Abort Command Limit (Maximum number of concurrently outstanding Abort commands) (0's based value)
259	M	3h	Asynchronous Event Request Limit (Maximum number of concurrently outstanding Asynchronous Event Request commands) (0's based value)
260	M	17h	FirmwareUpdates Bits7:5–Reserved Bits4– 1h Controller supports firmware activation without a reset 0h Controller requires a reset for firmware to be activated Bits3:1–Numbeorffirmwareslots Bit 0 – 1h Slot 1 is read only
261	M	3Eh	Log Page Attributes Bits 7:5 are reserved. Bit 4: Persistent Event log. Bit 3: the Telemetry Host-Initiated and Telemetry Controller-Initiated log pages and sending Telemetry Log Notices. Bit 2: extended data for the Get Log Page command. Bit 1: the Commands Supported and Effects log page. Bit 0: 0h SMART data is global for all namespaces
262	M	3Fh	Error Log Page Entries (Maximum number of Error Information log entries stored by controller) (0's based value)
263	M	1h	Number of Power States Support (0's based value)
264	M	1h	Admin Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates Admin Vendor Specific Commands use the format defined in Admin and NVM Vendor Specific Commands (Optional) table of NVM Express spec.
265	O	0h	Autonomous Power State Transition Attributes (APSTA)
267:266	M	15Eh	Warning Composite Temperature Threshold
269:268	M	166h	Critical Composite Temperature Threshold
271:270	O	Ah	Maximum Time for Firmware Activation
275:272	O	0h	Host Memory Buffer Preferred Size
279:276	O	0h	Host Memory Buffer Minimum Size

295:280	O	960GB: DF90356000h 1.92TB: 1BF1FC56000h 3.84TB: 37E3EE56000h 7.68TB:6FC7D256000h 15.36TB: DF880000000h	Total NVM Capacity
311:296	O	0h	Unallocated NVM Capacity
315:312	O	0h	Replay Protected Memory Block Support(RPMBS)
317:316	O	23h	Extended Device Self-test Time (EDSTT)
318	O	1h	Device Self-test Options (DSTO)
319	M	0h	Firmware Update Granularity (FWUG)
321:320	M	Ah	Keep Alive Support (KAS)
323:322	O	0h	Host Controlled Thermal Management Attributes (HCTMA)
325:324	O	0h	Minimum Thermal Management Temperature (MNTMT)
327:326	O	0h	Maximum Thermal Management Temperature (MXTMT)
331:328	O	40000003h	Sanitize Capabilities (SANICAP)
335:332	O	0h	Host Memory Buffer Minimum Descriptor Entry Size (HMMINDS)
337:336	O	0h	Host Memory Maximum Descriptors Entries (HMMAXD)
339:338	O	0h	NVM Set Identifier Maximum (NSETIDMAX)
341:340	O	0h	Endurance Group Identifier Maximum (ENDGIDMAX)
342	O	0h	ANA Transition Time (ANATT)
343	O	0h	Asymmetric Namespace Access Capabilities (ANACAP)
347:344	O	0h	ANA Group Identifier Maximum (ANAGRPMAX)
351:348	O	0h	Number of ANA Group Identifiers (NANAGRPID)
355:352	O	5h	Persistent Event Log Size (PELS):
357:356	O	0h	Domain Identifier:
367:358	-	-	Reserved
383:368	O	0h	Max. Endurance Group Capacity (MEGCAP)
511:384	-	-	Reserved
512	M	66h	Submission Queue Entry Size Bits 7:4 – 6h Max SQES (64 bytes) Bits 3:0 – 6h Required SQES (64 bytes)
513	M	44h	Completion Queue Entry Size Bits 7:4 – 4h Max SQES (16 bytes) Bits 3:0 – 4h Required SQES (16 bytes)
515:514	M	180h	Maximum Outstanding Commands (MAXCMD)
519:516	M	80h	Number of Namespaces
521:520	M	DFh	Optional NVM Command Support Bits 15:6 – Reserved Bit 5 – 1h Reservations Supported 0h Not support Reservations Bit 4 – 1h Save field in Set Feature & Select field in Get Feature Supported 0h Not support Save field in Set Feature & Select field in Get Feature Bit 3 – 1h Write Zeros Supported 0h Not support Write Zeros Bit 2 – 1h Dataset Management Supported 0h Not support Dataset Management Bit 1 – 1h Write Uncorrectable Supported 0h Not support Write Uncorrectable Bit 0 – 1h Compare Supported 0h Not support Compare
523:522	M	1h	Fused Operation Support Bits 15:1 – Reserved Bit 0 – 0h Compare/Write Fused Operation Not Supported

524	M	4h	Format NVM Attributes Bits 7:3 – Reserved Bit 2 – 1h Cryptographic Erase Bit 1 – 1h Secure Erase Per Namespace Bit 0 – 0h Format Per Namespace
525	M	6h	Volatile Write Cache 0h – No VWC present
527:526	M	1FFh	Atomic Write Unit Normal
529:528	M	7h	Atomic Write Unit Power Fail (0's based value)
530	M	1h	NVM Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates NVM Vendor Specific Commands use the format defined in NVM Express specification
531	M	1h	Namespace Write Protection Capabilities
533:532	O	7h	ACWU
535:534	M	0h	Reserved
539:536	O	F0001h	SGL support bit 21 Data Block bit 20 Offset bit 19 MPTR bit 18 Length Lager Transfer bit 17 metadata buffer alignment requirements bit 16 Supports SGL Bit Bucket descriptor bit 15:08 SGL Descriptor Threshold bit 2" Supports Keyed SGL Data Block descripto" bit 1:0 Supports SGL
543:540	O	80h	Maximum Number of Allowed Namespaces
599:544	O	80h	Maximum Domain Namespace Attachments
563:560	O	80h	Maximum I/O Controller Namespace Attachments
703:564	-	0h	Reserved
767:704	-	0h	Reserved
1023:768			NVM Subsystem NVMe™ Qualified Name (SUBNQN)
I/O Command Set Attributes			
1791:1024	-	0h	Reserved
2047:1792			Refer to the NVMe™ over Fabrics specification
Power State Descriptors			
2079:2048	M	Refer to 'Identify Power State Descriptor Data Structure'	Power State 6 Descriptor
3071:2080	O	0h	Power State 1 ~ 31 Descriptor (PSD1~N)
3072	O	3h	Error Mode Capabilities (ERRCAP)
3073	-	0h	Current Error Mode
3075:3074	O	137h	Supports Debugging Feature on Error Mode
3079:3076	O	0h	Reason for entering Error Mode.
3087:3080	O	84GRSUND	Option ROM Version
3091:3088	O	22200811h	Option ROM Build Date
3092	O	1h	OEM Extended SMART Supported
3278:3093			Reserved
3279	M	6h	Security Features Supported
Vendor Specific			
4095:3280	-	-	Samsung Reserved

[Table 137] Identify Power State Descriptor Data Structure

Bits	Description	Power State 0	Power State 1	Power State 2
255:184	Reserved			
183:182	Active Power Scale(APS)	2	2	2
181:179	Reserved			
178:176	Active Power Workload(APW)	2	2	2
175:160	Active Power(ACTP)	1700	1200	800
159:152	Reserved			
151:150	Idle Power Scale(IPS)	2	2	2
149:144	Reserved			
143:128	Idle Power(IDLP)	500	500	500
127:125	Reserved			
124:120	Relative Write Latency	0	1	1
119:117	Reserved			
116:112	Relative Write Throughput	0	1	1
111:109	Reserved			
108:104	Relative Read Latency	0	1	1
103:101	Reserved			
100:96	Relative Read Throughput	0	1	1
95:64	Exit Latency	160	160	160
36:32	Entry Latency	160	160	160
31:26	Reserved			
25	Non-Operational State	0	0	0
24	Max Power Scale	0	0	0
23:16	Reserved			
15:00	Maximum Power	2500	1200	800

[Table 138] Identify Namespace Data Structure

Bytes	O/M	Default Value	Description
7:00	M	960GB: 6FC81AB0h 1.92TB: DF8FE2B0h 3.84TB: 1BF1F72B0h 7.68TB: 37E3E92B0h 15.36TB: 6FC400000h	Namespace Size(512KB)
15:08	M	960GB: 6FC81AB0h 1.92TB: DF8FE2B0h 3.84TB: 1BF1F72B0h 7.68TB: 37E3E92B0h 15.36TB: 6FC400000h	Namespace Capacity(512KB)
23:16	M	0h	Namespace Utilization A device may report Namespace Utilization equal to Namespace Capacity at all times if the product is not targeted for thin provisioning environments
24	M	1Ah	Namespace Features Bits 7:5 are reserved. Bit 4 if set to '1' indicates that the fields NPWG, NPWA, NPDG, NPDA, and NOWS are defined for this namespace and should be used by the host for I/O optimization; and NOWS defined for this namespace shall adhere to Optimal Write Size field setting defined in NVM Sets Attributes Entry for the NVM Set with which this namespace is associated. If cleared to '0', the controller does not support the fields NPWG, NPWA, NPDG, NPDA, and NOWS for this namespace; and Optimal Write Size field in NVM Sets Attributes Entry for the NVM Set with which this namespace is associated should be used by the host for I/O optimization. Bit 3 if set to '1' indicates that the non-zero NGUID and non-zero EUI64 fields for this namespace are never reused by the controller. If cleared to '0', then the NGUID and EUI64 values may be reused by the controller for a new namespace created after this namespace is deleted. This bit shall be cleared to '0' if both NGUID and EUI64 fields are cleared to 0h. Refer to section 7.11. Bit 2 if set to '1' indicates that the controller supports the Deallocated or Unwritten Logical Block error for this namespace. If cleared to '0', then the controller does not support the Deallocated or Unwritten Logical Block error for this namespace. Refer to section 6.7.1.1. Bit 1 if set to '1' indicates that the fields NAWUN, NAWUPF, and NACWU are defined for this namespace and should be used by the host for this namespace instead of the AWUN, AWUPF, and ACWU fields in the Identify Controller data structure. If cleared to '0', then the controller does not support the fields NAWUN, NAWUPF, and NACWU for this namespace. In this case, the host should use the AWUN, AWUPF, and ACWU fields defined in the Identify Controller data structure in Figure 111. Refer to section 6.4. Bit 0 if set to '1' indicates that the namespace supports thin provisioning. Specifically, the Namespace Capacity reported may be less than the Namespace Size. When this feature is supported and the Dataset Management command is supported, then deallocating LBAs shall be reflected in the Namespace Utilization field. Bit 0 if cleared to '0' indicates that thin provisioning is not supported and the Namespace Size and Namespace Capacity fields report the same value
25	M	5h	Number of LBA Formats
26	M	0h	Formatted LBA Size Bits 7:5 – Reserved Bit 4 – Metadata interleaved or separate (based on LBA format) Bit 3:0 – Indicates LBA format
27	M	3h	Metadata Capabilities Bits 7:2 – Reserved Bit 1 – Supports Metadata as separate buffer Bit 0 – Supports Metadata as extended LBA
28	M	1Fh	End-to-end Data Protection Capabilities Bits 7:5 – Reserved Bit 4 – Supports protection information as last 8 bytes of Metadata Bit 3 – Supports protection information as first 8 bytes of metadata Bit 2 – Supports Type 3 protection information Bit 1 – Supports Type 2 protection information Bit 0 – Supports Type 1 protection information

29	M	0h	End-to-End Data Protection Type Settings Bits 7:4 – Reserved Bit 3 – 1: Protection information transferred as first 8 bytes of metadata Bit 3 – 0: Protection information transferred as last 8 bytes of metadata Bit 2:0 – 000b: Protection information disabled Bit 2:0 – 1h: Protection type 1 enabled Bit 2:0 – 2h: Protection type 2 enabled Bit 2:0 – 3h: Protection type 3 enabled
30	O	0h	Namespace Multi-path I/O and Namespace sharing Capabilities (NMIC) Bits 7:1 - Reserved Bit 0 - 1 : Accessible by two or more controllers Bit 0 - 0 : Private namespace
31	O	0h	Reservation Capabilities (RESCAP) Bits 7 - Reserved Bits 6 - 1: Namespace supports the Exclusive Access (All Registrants reservation type) Bit 5 - 1 : Namespace supports the Write Exclusive (All Registrants reservation type) Bit 4 - 1 : Namespace supports the Exclusive Access (Registrants only reservation type) Bit 3 - 1 : Namespace supports the Write Exclusive (Registrants only reservation type) Bit 2 - 1 : Namespace supports the Exclusive Access Reservation type Bit 1 - 1 : Namespace supports the Write Exclusive Reservation type Bit 0 - 1 : Namespace supports the Persist Through Power Loss capability
32	O	80h	Format Progress Indicator(FPI)
33	O	9h	Deallocate Logical Block Features (DLFEAT)
35:34	O	1FFh	Namespace Atomic Write Unit Normal
37:36	O	7h	Namespace Atomic Write Unit Power Fail
39:38	O	7h	Namespace Atomic Compare & Write Unit
41:40	O	1FFh	Namespace Atomic Boundary Size Normal
43:42	O	0h	Namespace Atomic Boundary Offset
45:44	O	7h	Namespace Atomic Boundary Size Power Fail
47:46	-	Reserved	
63:48	O	960GB: DF90356000h 1.92TB: 1BF1FC56000h 3.84TB: 37E3EE56000h 7.68TB:6FC7D256000h 15.36TB: DF880000000h	NVM Capacity (NVMCAP)
65:64	O	FFh	Namespace Preferred Write Granularity (NPWG)
67:66	O	7h	Namespace Preferred Write Alignment (NPWA)
69:68	O	FFh	Namespace Preferred Deallocate Granularity (NPDG)
71:70	O	7h	Namespace Preferred Deallocate Alignment (NPDA)
73:72	O	FFh	Namespace Optimal Write Size (NOWS)
99:74	O	0h	Reserved
101:100	O	0h	NVM Set Identifier (NVMSETID)
103:102	O	0h	Endurance Group Identifier (ENDGID)
119:104	O	Update by Vendor Command	Namespace Globally Unique Identifier (NGUID) #:Variables *NGUID specifies data in a big endian format.
127:120	O	0h	IEEE Extended Unique Identifier(EUI64) #:Variables *EUI64 specifies data in a big endian format
131:128	M	Refer to 'LBA Format 0 Data Structure'	LBA Format 0 Support
135:132	O	Refer to 'LBA Format 1 Data Structure'	LBA Format 1 Support
139:136	O	Refer to 'LBA Format 2 Data Structure'	LBA Format 2 Support
143:140	O	Refer to 'LBA Format 3 Data Structure'	LBA Format 3 Support
147:144	O	Refer to 'LBA Format 4 Data Structure'	LBA Format 4 Support
151:148	O	Refer to 'LBA Format 5 Data Structure'	LBA Format 5 Support

…			
191:188	O	0h	LBA Format 15 Support (N/A)
383:192	-	0h	Reserved
Vendor Specific			
4095:384	-	-	Samsung Reserved

[Table 139] LBA Format 0 Data Structure

Bits	Name	Default Value	Description
31:26	-	0h	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	9h	LBA Data Size
15:00	MS	0h	Metadata Size

[Table 140] LBA Format 1 Data Structure

Bits	Name	Default Value	Description
31:26	-	0h	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	9h	LBA Data Size
15:00	MS	8h	Meta data Size

[Table 141] LBA Format 2 Data Structure

Bits	Name	Default Value	Description
31:26	-	0h	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	Ch	LBA Data Size
15:00	MS	0h	Meta data Size

[Table 142] LBA Format 3 Data Structure

Bits	Name	Default Value	Description
31:26	-	0h	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	Ch	LBA Data Size
15:00	MS	8h	Meta data Size

[Table 143] LBA Format 4 Data Structure

Bits	Name	Default Value	Description
31:26	-	0h	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	Ch	LBA Data Size
15:00	MS	10h	Meta data Size

.

[Table 144] LBA Format 5 Data Structure

Bits	Name	Default Value	Description
31:26	-	0h	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	Ch	LBA Data Size
15:00	MS	40h	Meta data Size

6.2 NVM Express™ I/O Command Set

[Table 145] Opcode for NVM Express™ I/O Commands

Opcode (Hex)	Command Name
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management
0Ch	Verify

NOTE: 1) Deallocate feature in Dataset Management command is only supported in the Samsung SSD PM9D3a.

6.3 SMART/Health Information

[Table 146] SMART/Health Information Log

Bytes	Default Value	Attribute Description
0	0	Critical Warning Bit 7:5 – Reserved Bit 4 – 1h: the volatile memory backup device has failed. (only valid if the controller has a volatile memory backup solution) Bit 3 – 1h: the media has been placed in read only mode Bit 2 – 1h: the device reliability has been degraded due to significant media related errors or any internal error that degrades device reliability Bit 1 – 1h: the temperature has exceeded a critical threshold Bit 0 – 1h: the available spare space has fallen below the threshold
2:1	Current Temperature	Temperature (composite temperature)
3	100	Available Spare
4	10	Available Spare Threshold
5	0	Percentage Used
6	-	Endurance Group Critical Warning Summary
31:7	-	Reserved
47:32	0	Data Units Read
63:48	0	Data Units Written
79:64	0	Host Read Commands
95:80	0	Host Write Commands
111:96	0	Controller Busy Time
127:112	0	Power Cycles
143:128	0	Power On Hours
159:144	0	Unsafe Shutdowns
175:160	0	Media Errors
191:176	0	Number of Error Information Log Entries
195:192	-	Warning Composite Temperature Time
199:196	0	Critical Composite Temperature Time
201:200	Current Temperature	Temperature Sensor 1
203:202	Current Temperature	Temperature Sensor 2
205:204	-	Temperature Sensor 3
207:206	-	Temperature Sensor 4
209:208	-	Temperature Sensor 5
211:210	-	Temperature Sensor 6
213:212	-	Temperature Sensor 7
215:213	-	Temperature Sensor 8

219:216	-	Thermal Management Temperature 1 Transition Count
223:220	-	Thermal Management Temperature 2 Transition Count
227:224	-	Total Time For Thermal Management Temperature 1
231:228	-	Total Time For Thermal Management Temperature 2
511:216	-	Reserved

6.4 Extended SMART Information

[Table 147] Specific Smart Log Additional (LID: 0xCA)

Bytes	Default Value	Attribute Description
0	ABh	Program fail count
2:1	0	Reserved
3	64h	Normalized value
4	0	Reserved
11:5	0	Current Raw value
12	ACh	Erase fail count
13	0	Reserved
15	64h	Normalized value
16	0	Reserved
23:17	0	Current Raw value
24	ADh	Wear Leveling count
26:25	0	Reserved
27	64h	Normalized value
28	0	Reserved
35:29	0	Current Raw value
36	B8h	End to End Error count
38:37	0	Reserved
39	64h	Normalized value
40	0	Reserved
47:41	0	Current Raw value
48	C7h	CRC error count
50:49	0	Reserved
51	64h	Normalized value
52	0	Reserved
59:53	0	Current Raw value
60	E2h	Timed workload, media wear
62:61	0	Reserved
63	64h	Normalized value
64	0	Reserved
71:65	0	Current Raw value
72	E3h	Timed workload, host read%
74:73	0	Reserved
75	64h	Normalized value
76	0	Reserved
83:77	0	Current Raw value
84	E4h	Timed workload,Timer
86:85	0	Reserved
87	64h	Normalized value
88	0	Reserved
95:89	0	Current Raw value
96	EAh	Thermal Throttle Status
98:97	0	Reserved
99	64h	Normalized value
100	0	Reserved
107:101	0	Current Raw value
119:108	Always '0'	Lifetime Retry Buffer Overflow Count

131:120	Always '0'	PLL Lock Loss Count
132	F4h	NAND Bytes written
134:133	0	Reserved
135	64h	Normalized value
136	0	Reserved
143:137	0	Current Raw value
144	F5h	Host Bytes written
146:145	0	Reserved
147	64h	Normalized value
148	0	Reserved
155:149	0	Current Raw value
156	FCh	Xor Pass count
158:157	0	Reserved
159	64h	Normalized value
160	0	Reserved
166:161	0	Current Raw value
167	0	Reserved
168	FDh	Xor Fail count
170:169	0	Reserved
171	64h	Normalized value
172	0	Reserved
178:173	0	Current Raw value
179	0	Reserved
180	FEh	Xor Invoked count
182:181	0	Reserved
183	64h	Normalized value
184	0	Reserved
190:185	0	Current Raw value
191	0	Reserved
197:192	Always '0'	In-flight Read IO CMD
203:198	Always '0'	In-flight Write IO CMD
255:204	-	Reserved
259:256	0	Lifetime Write Amplification Factor
263:260	0	Trailing Hour Write Amplification Factor
279:264	0	Lifetime user writes Track the number of user data written by the host.
295:280	0	Lifetime NAND writes Track number of data written by the controller to the NAND
311:296	0	Lifetime user reads Track the number of user data read by the host
315:312	0	Lifetime retired block count Count of number of blocks that have been reallocated
317:316	Current temperature	Current Temperature
319:318	-	Reserved
323:320	reserved block count	Lifetime Unused Reserved Block
331:324	0	Lifetime read Reclaim count
339:332	0	Lifetime UECC count
343:340	0	Lifetime Used Reserved Block
359:344	0	Power on hours
375:360	0	Lifetime clean shutdown count on power loss(NPO count)
391:376	0	Lifetime unclean shutdowns on power loss(SPO count)
395:392	0	Perf Indicator
399:396	0	WearLevel Count
403:400	0	HW Error Type

407:404	-	Reserved
411:408	0	CoreSRAM CECC Count
415:412	0	CoreSRAM CECC Address
419:416	0	BufferSRAM CECC Count
423:420	0	BufferSRAM CECC Address
427:424	0	DRAM CECC Count
435:428	0	DRAM CECC Address
439:436	0	DRAM UECC Count
447:440	0	DRAM UECC Address
451:448	0	E2E Error Count
453:452	0	FW Update Success Count
455:454	0	FW Update Fail Count
471:456	-	Reserved
479:472	0	Reset Count
495:480	0	Trimmed Sector Count
499:496	0	Security Meta Erase Fail Count
503:500	0	Over Temperature Count
507:504	0	Under Temperature Count
511:508	0	Recovery Reset Count

[Table 148] Enhanced SMART Information Log (LID: 0xC4)

Bytes	Default Value	Attribute Description
1:0	0	Throughput Performance
2:2	0	Timed workload Media Wear
3:3	0x64	Timed workload Host Read/Write Ratio
5:4	0	Read Error Rate
7:6	Always '0'	Write Error Rate
11:8	Always '0'	Unrecoverable Write Errors
15:12	0	Read Recovery Attempts
17:16	temperature	Average Short Term temperature
19:18	temperature	Average Long Term temperature
21:20	temperature	Highest temperature
23:22	temperature	Lowest temperature
25:24	0	Highest average Short Term temperature
27:26	0	Lowest average Short Term temperature
29:28	0	Highest average Long Term temperature
31:30	0	Lowest average Long Term temperature
33:32	0x15E	Specified maximum operating temperature
35:34	0x111	Specified minimum operating temperature
39:36	0	Time in Over Temperature in minutes
153:40	-	Reserved
157:154	0	BAD TLP Count
161:158	0	BAD DLLP Count
165:162	0	PHY Error Count
169:166	0	Thermal Protection Count
173:170	0	Thermal Shutdown Count
177:174	0	Latency Spike Trigger Count
181:178	0	Conditional Dump Trigger Count
511:182	-	Reserved

[Table 149] Enhanced SMART Information Log (LID: 0xD0)

Bytes	Default Value	Attribute Description
0	0xD0	Log Page ID
4:1	0x0200 (‘512’)	Log Page Size
5:5	0x30	Log Page Version
21:6	0x03FA28C91DD3406BB9CBBE3680C5D2ED	Log Page GUID
22:22	0	Patch Version
31:23	-	Reserved
35:32	Always '0'	EPI Count
36:36	0	Min EC Meta Block Used
37:37	0	Max EC Meta Block Used
38:38	0	Avg EC Meta Block Used
54:39	0	Thermal Throttling Write Total
70:55	0	Thermal Throttling Read Total
90:71	0	Recovery Count
94:91	0	Erase Fail Block Count
98:95	0	Program Fail Block Count
102:99	0	Read Fail Block Count
110:103	0	Read Recovery Count
114:111	0	Patrol Read Reclaim Count
118:115	0	Fast Cycle Count
122:119	0	Deep Erase Count
126:123	0	Blocking GC Count on Run-time
130:127	0	Blocking GC Count during Power-on
132:131	-128	Controller Max Temperature
134:133	127	Controller Min Temperature
135:135	Always '0'	Turbo write enable status
136:136	Always '0'	Turbo status
232:137	0	EQ phase2 PRESET history
328:233	0	EQ phase3 PRESET history
344:329	0	Gen3 EQ phase3 Coefficient history
360:345	0	Gen4 EQ phase3 Coefficient history
376:361	0	Gen5 EQ phase3 Coefficient history
511:377	-	Reserved

[Table 150] Cloud Attribute Log Page (LID : 0xC0) OCP Spec 2.0

Bytes	Default Value	Attribute Description
15:0	0	Physical Media Units Written
31:16	0	Physical Media Units Read
39:32	0	Bad User NAND block count
47:40	0	Bad System NAND block count
55:48	0	XOR Recovery count
63:56	0	Uncorrectable read error count
71:64	0	Soft ECC error count
79:72	0	End to End Correction Counts
80:80	0	System data % used
87:81	0	Refresh Counts
95:88	0	User data erase counts
97:96	0	Thermal throttling status and count
103:98	-	Reserved
111:104	0	PCIe Correctable Error count
115:112	0	Incomplete Shutdowns
119:116	-	Reserved
120:120	0x64	% Free Blocks
127:121	-	Reserved
129:128	Capacitor Health	Capacitor Health
135:130	-	Reserved
143:136	0	Unaligned I/O
151:144	[147:144] Security Version : 0x0 [151:148] Blocking FW Image Version : 0x0	Security Version Number
159:152	0	NUSE
175:160	0	PLP Start Count
191:176	device capacity specific	Endurance Estimate
493:192	-	Reserved
495:494	0x3	Log Page Version
511:496	0xAFD514C97C6F4F9CA4f2BFEA2810AFC5	Log Page GUID

7.0 SPOR SPECIFICATION (Sudden Power Off and Recovery)

7.1 Data Recovery in Sudden Power off

If power interruption is detected, SSD dumps all cached user data and meta data to NAND Flash.
SSD could protect even the user data in DRAM from sudden power off while SSD is used with cache on.
Commonly, data is protected all of the operation period.

7.2 Minimum Off Time

In sudden power off case, minimum 10ms off time is required for stability.

7.3 Time to Ready Sequence

In normal power-off recovery status, SSD needs less than 960GB/1.92TB/1.6TB/3.84TB/3.2TB 8seconds, 7.68TB/6.4TB 15seconds, 15.36TB/12.8TB 20seconds to reach operating mode where SSD works perfectly with cache-on state.
SSD is ready to respond identify Device command during FTL OPEN.
When the sudden power-off occurs, the user data in DRAM will be dumped into the NAND Flash using the stored power in the capacitor.
In sudden power-off recovery condition, mapping data will be loaded or the FTL meta data be rebuilt perfectly for initial max.10 seconds.
During this period, Identify Device command is still supported. It is called SPOR. (Sudden Power Off and Recovery)

[Table 151] Device Ready Time for Normal Read / Write Operation after Sudden Power Off

	960GB/1.92TB/1.6TB/3.84TB/3.2TB	7.68TB/6.4TB	15.36TB/12.8TB
Max. Open Time (sec)	8s	15s	20s

8.0 SMBUS RESOURCES

The expansion ROM integrated in Samsung SSD PM9D3a supports booting UEFI operating system installed on the drive, it complies to UEFI standard, which is specified in UEFI v2.4 Specification.

This section listed data structures and registers accessible through SMBus interface.
Vital Product Data (VPD) is stored in SM-Bus slave address of 0xA6 (bits 7-1 correspond to 1010_011 on the SM-Bus). Temperature sensor is stored in SM-Bus slave address of 0x36 (bits 7-1 correspond to 0011_011).
Data offset of VPD EEPROM is 1Byte(8bit)

8.1 Temperature sensor data Structure

Temperaure sensor data(SM-Bus slave address of 0x36) information are shown as below.

The 16-bit value is 2s complement representation of a temperature with the Bit 4 equal to the minimum granularity of 1 °C. Bit 12 is the sign bit.
For example, the value of 0190h represents 25 °C, the value of 07C0 h represents 124 °C, and the value of 1E80 h represents -24 °C

By choosing the starting of the lowest bit the resolution of the temperature sensor can be defined. Temperature sensor is at resolution of 1°C (8-bit)

B15/B07	B14/B06	B13/B05	B12/B04	B11/B03	B10/B02	B09/B01	B08/B00
N/A	N/A	N/A	Sign	128	64	32	16
8	4	2	1	N/A	N/A	N/A	N/A

8.2 Temperature Sensor Register Summary

Offset	Type	Name	Description	Default
00	RO	Capabilities	Capability register	0x00EF
01	RW	Configuration	Configuration register (CONFIG)	0x0000
02	RW	TUPPER	Event Temperature Upper-Boundary Trip register	0x0000
03	RW	TLOWER	Event Temperature Lower-Boundary Trip register	0x0000
04	RW	TCRIT	Critical Temperature Trip register	0x0000
05	RO	TA	Ambient Temperature	0x0000
06	RO	Manufacture ID	Manufacturer ID register	0x0054
07	RO	Reserved	Reserved	0x0601
08	RO	Device/Revision	Device ID/Revision register	0x0601
09	RW	Resolution register	Resolution register	0x0001

8.2.1 Capability register

Bits	Type	Default Value	Description
15:8	RO	0	Unimplemented: Read as '0'
7	RO	1	Event Output Status During Shutdown (SHDN Status): 0 = Event output remains in previous state. If the output asserts before shutdown command, it remains asserted during shutdown. 1 = Event output deasserts during shutdown. After shutdown, it takes tCONV to reassert the event output (power-up default)
6	RO	1	I2C Bus Time-Out (tOUT Range): 0 = Bus time-out range is 10 ms to 60 ms 1 = Bus time-out range is 25 ms to 35 ms (power-up default)
5	RO	1	Unimplemented: Read as '1'
4:3	RO	1	Resolution: 00 = 0.5°C 01 = 0.25°C (power-up default) 10 = 0.125°C 11 = 0.0625°C
2	RO	1	Temperature Measurement Range (Meas. Range): 0 = TA=0 (decimal) for temperature below 0°C 1 = The part can measure temperature below 0°C (power-up default)
1	RO	1	Accuracy: 0 = Accuracy → ±2°C from +75°C to +95°C (Active Range) and ±3°C from +40°C to +125°C (Monitor Range) 1 = Accuracy → ±1°C from +75°C to +95°C (Active Range) and ±2°C from +40°C to +125°C (Monitor Range)
0	RO	1	Temperature Alarm: 0 = No defined function (This bit will never be cleared or set to '0') 1 = The part has temperature boundary trip limits (TUPPER/TLOWER/TCRIT registers) and a temperature event output (JC 42.4 required feature)

8.2.2 Configuration register (CONFIG)

Bits	Type	Default Value	Description
15:11	RW	0	Unimplemented: Read as '0'
10:9	RW	00	TUPPER and TLOWER Limit Hysteresis (THYST): 00 = 0°C (power-up default) 01 = 1.5°C 10 = 3.0°C 11 = 6.0°C
8	RW	0	Shutdown Mode (SHDN): 0 = Continuous Conversion (power-up default) 1 = Shutdown (Low-Power mode)
7	RW	0	TCRIT Lock Bit (Crit. Lock): 0 = Unlocked. TCRIT register can be written. (power-up default) 1 = Locked. TCRIT register can not be written
6	RW	0	TUPPER and TLOWER Window Lock Bit (Win. Lock): 0 = Unlocked. TUPPER and TLOWER registers can be written. (power-up default) 1 = Locked. TUPPER and TLOWER registers can not be written
5	RW	0	Interrupt Clear (Int. Clear) Bit: 0 = No effect (power-up default) 1 = Clear interrupt output. When read this bit returns '0'
4	RW	0	Event Output Status (Event Stat.) Bit: 0 = Event output is not asserted by the device (power-up default) 1 = Event output is asserted as a comparator/Interrupt or critical temperature output
3	RW	0	Event Output Control (Event Cnt.) Bit: 0 = Event output Disabled (power-up default) 1 = Event output Enabled
2	RW	0	Event Output Select (Event Sel.) Bit: 0 = Event output for TUPPER, TLOWER and TCRIT (power-up default) 1 = TA ≥ TCRIT only. (TUPPER and TLOWER temperature boundaries are disabled.)
1	RW	0	Event Output Polarity (Event Pol.) Bit: 0 = Active-low (power-up default. Pull-up resistor required) 1 = Active-high
0	RW	0	Event Output Mode (Event Mod.) Bit: 0 = Comparator output (power-up default) 1 = Interrupt output

8.2.3 Event Temperature, Critical Temperature Trip register

Bits	Type	Default Value	Description	Remark
15:13	RW	0	Unimplemented: Read as '0'	
12	RW	0	Sign: 0 = TA ≥ 0°C 1 = TA < 0°C	
11	RW	0	2^{7}°C	TUPPER/TLOWER/TCRIT: Temperature boundary trip data in two's complement format
10	RW	0	2^{6}°C	
09	RW	0	2^{5}°C	
08	RW	0	2^{4}°C	
07	RW	0	2^{3}°C	
06	RW	0	2^{2}°C	
05	RW	0	2^{1}°C	
04	RW	0	2^{0}°C	
03	RW	0	2^{-1}°C	
02	RW	0	2^{-2}°C	
1:0	RW	0	Unimplemented: Read as '0'	

8.2.4 Ambient Temperature Register

Bits	Type	Default Value	Description
15	RO	0	TA vs. TCRIT Bit: 0 = TA < TCRIT°C 1 = TA ≥ TCRIT°C
14	RO	0	TA vs. TUPPER Bit: 0 = TA ≤ TUPPER°C 1 = TA > TUPPER°C
13	RO	0	TA vs. TLOWER Bit: 0 = TA ≥ TLOWER°C 1 = TA < TLOWER°C
12	RO	0	Sign: 0 = TA ≥ 0°C 1 = TA < 0°C
11	RO	0	2^{7}°C
10	RO	0	2^{6}°C
09	RO	0	2^{5}°C
08	RO	0	2^{4}°C
07	RO	0	2^{3}°C
06	RO	0	2^{2}°C
05	RO	0	2^{1}°C
04	RO	0	2^{0}°C
03	RO	0	2^{-1}°C
02	RO	0	2^{-2}°C
01	RO	0	2^{-3}°C
0	RO	0	2^{-4}°C

8.2.5 Manufacture ID Register

Bits	Type	Default Value	Description
15:0	RO	0x0054	Device Manufacturer Identification Number

8.2.6 Device/Revision Register

Bits	Type	Default Value	Description
15:0	RO	0x0601	Device ID / Revision Register

8.2.7 Resolution Register

Bits	Type	Default Value	Description
15	RW	0	Unimplemented: Read as '0'
14:2	RO	0	Unimplemented: Read as '0'
1:0	RW	01	Resolution: 00 = LSb = 0.5°C (tCONV = 30 ms, typical) 01 = LSb = 0.25°C (power-up default, tCONV = 65 ms, typical) 10 = LSb = 0.125°C (tCONV = 130 ms, typical) 11 = LSb = 0.0625°C (tCONV = 260 ms, typical)

8.3 Vital Product Data(VPD) Structure

VPD(SM-Bus slave address of 0xA6) listed device specific information for Enterprise PCIe® SSD discovery and power allocation.
Compliant with NVM Express™ Management Interface, Revision 1.2.

[Table 152] VPD Information

Total Bytes (Decimal)	Total Bytes (Hex-Dec)	Byte Offset (Decimal)	Size bytes	Name		960GB	1.92TB	3.84TB	7.68TB	15.36TB
0	0	0	1	Common Header	IPMI Format Version Number (IPMIVER)	01	01	01	01	01
1	1	1	1		Internal Use Area Starting Offset	00	00	00	00	00
2	2	2	1		Chassis Info Area Starting Offset (CIAOFF)	00	00	00	00	00
3	3	3	1		Board Info Area Starting Offset (BIAOFF)	00	00	00	00	00
4	4	4	1		Product Info Area Starting Offset (PIAOFF)	01	01	01	01	01
5	5	5	1		MultiRecord Info Area Starting Offset (MRIOFF)	0F	0F	0F	0F	0F
6	6	6	1		Reserved (00h)	00	00	00	00	00
7	7	7	1		Common Header Checksum	EF	EF	EF	EF	EF
8	8	0	1	Product info Area	IPMI Format Version Number	01	01	01	01	01
9	9	1	1		Product Info Area Length	0E	0E	0E	0E	0E
10	A	2	1		Language Code(19h=ENG)	19	19	19	19	19
11	B	3	1		Manufacturer Name Type/ Length	C8	C8	C8	C8	C8
12	C	4	1		Manufacturer Name (8 byte ASCII) **[Samsung]**	53	53	53	53	53
13	D	5	1			61	61	61	61	61
14	E	6	1			6D	6D	6D	6D	6D
15	F	7	1			73	73	73	73	73
16	10	8	1			75	75	75	75	75
17	11	9	1			6E	6E	6E	6E	6E
18	12	10	1			67	67	67	67	67
19	13	11	1			0	0	0	0	0
20	14	12	1		Product Name Type/Length	D8	D8	D8	D8	D8
21	15	13	1		Product Name (PNAME) Product Name (24byte ASCII) This should be correspond to that in the PCI Subsystem Vendor ID(SSVID) and IEEE OUI Identifier fields in the Identify Controller Data Structure **[PM9D3a]**	50	50	50	50	50
22	16	14	1			4D	4D	4D	4D	4D
23	17	15	1			39	39	39	39	39
24	18	16	1			44	44	44	44	44
25	19	17	1			33	33	33	33	33
26	1A	18	1			61	61	61	61	61
27	1B	19	1			0	0	0	0	0
28	1C	20	1			0	0	0	0	0
29	1D	21	1			0	0	0	0	0
30	1E	22	1			0	0	0	0	0
31	1F	23	1			0	0	0	0	0
32	20	24	1			0	0	0	0	0
33	21	25	1			0	0	0	0	0
34	22	26	1			0	0	0	0	0
35	23	27	1			0	0	0	0	0

36	24	28	1	Product info Area	Product Name (24byte ASCII) This should be correspond to that in the PCI Subsystem Vendor ID(SSVID) and IEEE OUI Identifier fields in the Identify Controller Data Structure **[PM9D3a]**	0	0	0	0	0
37	25	29	1			0	0	0	0	0
38	26	30	1			0	0	0	0	0
39	27	31	1			0	0	0	0	0
40	28	32	1			0	0	0	0	0
41	29	33	1			0	0	0	0	0
42	2A	34	1			0	0	0	0	0
43	2B	35	1			0	0	0	0	0
44	2C	36	1			0	0	0	0	0
45	2D	37	1		Product Part/Model Number Type/Length	E8	E8	E8	E8	E8
46	2E	38	1		Product Part/Model Number (40byte ASCII) **[960GB: SAMSUNG MZWL6960HFJA-00B07 1.92TB: SAMSUNG MZWL61T9HFLT-00B07 3.84TB: SAMSUNG MZWL63T8HFLT-00B07 7.68TB: SAMSUNG MZWL67T6HBLC-00B07 15.36TB: SAMSUNG MZWL615THBLF-00B07]**	53	53	53	53	53
47	2F	39	1			41	41	41	41	41
48	30	40	1			4D	4D	4D	4D	4D
49	31	41	1			53	53	53	53	53
50	32	42	1			55	55	55	55	55
51	33	43	1			4E	4E	4E	4E	4E
52	34	44	1			47	47	47	47	47
53	35	45	1			20	20	20	20	20
54	36	46	1			4D	4D	4D	4D	4D
55	37	47	1			5A	5A	5A	5A	5A
56	38	48	1			57	57	57	57	57
57	39	49	1			4C	4C	4C	4C	4C
58	3A	50	1			36	36	36	36	36
59	3B	51	1			39	31	33	37	31
60	3C	52	1			36	54	54	54	35
61	3D	53	1			30	39	38	36	54
62	3E	54	1			48	48	48	48	48
63	3F	55	1			46	46	46	42	42
64	40	56	1			4A	4C	4C	4C	4C
65	41	57	1			41	54	54	43	46
66	42	58	1			2D	2D	2D	2D	2D
67	43	59	1			30	30	30	30	30
68	44	60	1			30	30	30	30	30
69	45	61	1			42	42	42	42	42
70	46	62	1			30	30	30	30	30
71	47	63	1			37	37	37	37	37
72	48	64	1			0	0	0	0	0
73	49	65	1			0	0	0	0	0
74	4A	66	1			0	0	0	0	0
75	4B	67	1			0	0	0	0	0
76	4C	68	1			0	0	0	0	0
77	4D	69	1			0	0	0	0	0
78	4E	70	1			0	0	0	0	0
79	4F	71	1			0	0	0	0	0
80	50	72	1			0	0	0	0	0
81	51	73	1			0	0	0	0	0

82	52	74	1	Product info Area	Product Part/Model Number (40byte ASCII)	0	0	0	0	0
83	53	75	1			0	0	0	0	0
84	54	76	1			0	0	0	0	0
85	55	77	1			0	0	0	0	0
86	56	78	1		Product Version Type/Length	C2	C2	C2	C2	C2
87	57	79	1		Product Version (2 byte ASCII)	00	00	00	00	00
88	58	80	1			00	00	00	00	00
89	59	81	1		Product Serial Number Type/ Length	D4	D4	D4	D4	D4
90	5A	82	1		Product Serial Number (20byte ASCII)	0	0	0	0	0
91	5B	83	1			0	0	0	0	0
92	5C	84	1			0	0	0	0	0
93	5D	85	1			0	0	0	0	0
94	5E	86	1			0	0	0	0	0
95	5F	87	1			0	0	0	0	0
96	60	88	1			0	0	0	0	0
97	61	89	1			0	0	0	0	0
98	62	90	1			0	0	0	0	0
99	63	91	1			0	0	0	0	0
100	64	92	1			0	0	0	0	0
101	65	93	1			0	0	0	0	0
102	66	94	1			0	0	0	0	0
103	67	95	1			0	0	0	0	0
104	68	96	1			0	0	0	0	0
105	69	97	1			0	0	0	0	0
106	6A	98	1			0	0	0	0	0
107	6B	99	1			0	0	0	0	0
108	6C	100	1			0	0	0	0	0
109	6D	101	1			0	0	0	0	0
110	6E	102	1		Asset Tag Type/Length	00	00	00	00	00
111	6F	103	1		FRU File ID Type/Length	00	00	00	00	00
112	70	104	1		End of Record	C1	C1	C1	C1	C1
113	71	105	1		Reserved	00	00	00	00	00
114	72	106	1			00	00	00	00	00
115	73	107	1			00	00	00	00	00
116	74	108	1			00	00	00	00	00
117	75	109	1			00	00	00	00	00
118	76	110	1			00	00	00	00	00
119	77	111	1		Product Info Area CheckSum(0~110)					
120	78	0	1	NVMe™ MultiRecord Area	Record Type ID	0B	0B	0B	0B	0B
121	79	1	1		Record Format	02	02	02	02	02
122	7A	2	1		Record Length	3B	3B	3B	3B	3B
123	7B	3	1		Record Checksum(5~end)	BF	BF	BF	BD	3C
124	7C	4	1		Header Checksum (0~04)	F9	F9	F9	FB	7C
125	7D	5	1		NVMe™ MultiRecord Area Version Number:	00	00	00	00	00
126	7E	6	1		Management Endpoint Form Factor (MEFF)	11	11	11	11	11

127	7F	7	1	NVMe™ MultiRecord Area	MEFF reference 2.5" U.2 = 11h (15mmT) 2.5" U.2 = 12h (7mmT) 2.5" U.3 = 13h (15mmT) 2.5" U.3 = 14h (7mmT) M.2 22x110 = 35h M.2 22x80 = 34h 1U Short Form Factor - (SFF-TA-1006) 5.9 mm - 51h 1U Short Form Factor - (SFF-TA-1006) 8 mm - 52h 1U Long Form Factor - (SFF-TA-1007) 9.5 mm - 53h	00	00	00	00	00
128	80	8	1			00	00	00	00	00
129	81	9	1			00	00	00	00	00
130	82	10	1			00	00	00	00	00
131	83	11	1			00	00	00	00	00
132	84	12	1			00	00	00	00	00
133	85	13	1		Initial 1.8V Power Supply Requirements	00	00	00	00	00
134	86	14	1		Maximum 1.8V Power Supply Requirements:	00	00	00	00	00
135	87	15	1		Initial 3.3V Power Supply Requirements:	00	00	00	00	00
136	88	16	1		Maximum 3.3V Power Supply Requirements:	00	00	00	00	00
137	89	17	1		Reserved	00	00	00	00	00
138	8A	18	1		Maximum 3.3V aux Power Supply Requirements:	02	02	02	02	02
139	8B	19	1		Initial 5V Power Supply Requirements:	00	00	00	00	00
140	8C	20	1		Maximum 5V Power Supply Requirements:	00	00	00	00	00
141	8D	21	1		Initial 12V Power Supply Requirements:	0A	0A	0A	0A	0A
142	8E	22	1		Maximum 12V Power Supply Requirements:	10	10	10	11	11
143	8F	23	1		Maximum Thermal Load:	10	10	10	11	11
					LBA count	1875385008	3750748848	7501476528	1500293188	30001856512
					DEC to HEX	DF903560	1BF1FC560	37E3EE560	6FC7D2560	DF8800000
144	90	24	1		Total NVM Capacity(byte) - This field shoud correspond to the value reported in the TNV-CAP field in the NVMe™ Identify Controller Data Structure.	00	00	00	00	00
145	91	25	1			60	60	60	60	00
146	92	26	1			35	C5	E5	25	00
147	93	27	1			90	1F	3E	7D	80
148	94	28	1			DF	BF	7E	FC	F8
149	95	29	1			00	1	3	6	D
150	96	30	1			00	00	00	00	00
151	97	31	1			00	00	00	00	00
152	98	32	1			00	00	00	00	00
153	99	33	1			00	00	00	00	00
154	9A	34	1			00	00	00	00	00
155	9B	35	1			00	00	00	00	00
156	9C	36	1			00	00	00	00	00
157	9D	37	1		Reserved	00	00	00	00	00
158	9E	38	1			00	00	00	00	00
159	9F	39	1			00	00	00	00	00
160	A0	40	1			00	00	00	00	00
161	A1	41	1			00	00	00	00	00
162	A2	42	1			00	00	00	00	00
163	A3	43	1			00	00	00	00	00

164	A4	44	1	NVMe™ MultiRecord Area	Reserved	00	00	00	00	00
165	A5	45	1			00	00	00	00	00
166	A6	46	1			00	00	00	00	00
167	A7	47	1			00	00	00	00	00
168	A8	48	1			00	00	00	00	00
169	A9	49	1			00	00	00	00	00
170	AA	50	1			00	00	00	00	00
171	AB	51	1			00	00	00	00	00
172	AC	52	1			00	00	00	00	00
173	AD	53	1			00	00	00	00	00
174	AE	54	1			00	00	00	00	00
175	AF	55	1			00	00	00	00	00
176	B0	56	1			00	00	00	00	00
177	B1	57	1			00	00	00	00	00
178	B2	58	1			00	00	00	00	00
179	B3	59	1			00	00	00	00	00
180	B4	60	1			00	00	00	00	00
181	B5	61	1			00	00	00	00	00
182	B6	62	1			00	00	00	00	00
183	B7	63	1			00	00	00	00	00
184	B8	0	1	PCIe® Port MultiRecord Area	NVMe™ PCIe® Port Record Type ID	0C	0C	0C	0C	0C
185	B9	1	1		End of List / Record Format (end + 2h)	02	02	02	02	02
186	BA	2	1		Record Length (RLEN):	0B	0B	0B	0B	0B
187	BB	3	1		Record Checksum(5~end)	D9	D9	D9	D9	D9
188	BC	4	1		Header Checksum(0~4)	E	E	E	E	E
189	BD	5	1		NVMe™ PCIe® Port MultiRecord Area Version Number:	01	01	01	01	01
190	BE	6	1		PCIe® Port Number	00	00	00	00	00
191	BF	7	1		Port Information	01	01	01	01	01
192	C0	8	1		PCIe® Link Speed	1F	1F	1F	1F	1F
193	C1	9	1		PCIe® Maximum Link Width	04	04	04	04	04
194	C2	10	1		MCTP Support	01	01	01	01	01
195	C3	11	1		Ref Clk Capability	01	01	01	01	01
196	C4	12	1		Port Identifier (NVMe™-MI Port Identifier)	00	00	00	00	00
197	C5	13	1		Reserved	00	00	00	00	00
198	C6	14	1			00	00	00	00	00
199	C7	15	1			00	00	00	00	00

200	C8	0	1	Topology MultiRecord Area	Topology Record Type ID	0D	0D	0D	0D	0D
201	C9	1	1		Record Format	82	82	82	82	82
202	CA	2	1		Record Length (RLEN)	15	15	15	15	15
203	CB	3	1		Record Checksum(5 ~ end)	C4	C4	C4	C4	C4
204	CC	4	1		Header Checksum(0 ~ 4)	98	98	98	98	98
205	CD	5	1		Version Number	00	00	00	00	00
206	CE	6	1		Reserved	00	00	00	00	00
207	CF	7	1		Element Count	02	02	02	02	02
208	D0	8	1		NVM Subsystem Element - Type	07	07	07	07	07
209	D1	9	1		NVM Subsystem Element - Revision	00	00	00	00	00
210	D2	10	1		NVM Subsystem Element - Length	C	C	C	C	C
211	D3	11	1		NVM Subsystem Element - SMBus/I2C Address Info	3B	3B	3B	3B	3B
212	D4	12	1		NVM Subsystem Element - SMBus/I2C Capabilities	82	82	82	82	82
213	D5	13	1		NVM Subsystem Element - Port Descriptor Count	01	01	01	01	01
214	D6	14	1		NVM Subsystem Port Descriptor - Type	00	00	00	00	00
215	D7	15	1		NVM Subsystem Port Descriptor - Length	06	06	06	06	06
216	D8	16	1		NVM Subsystem Port Descriptor - PCIe® Link Speed	1F	1F	1F	1F	1F
217	D9	17	1		NVM Subsystem Port Descriptor - PCIe® Maximum Link Width	04	04	04	04	04
218	DA	18	1		NVM Subsystem Port Descriptor - RefClk Capability	01	01	01	01	01
219	DB	19	1		NVM Subsystem Port Descriptor - Port Identifier	00	00	00	00	00
220	DC	20	1		FRU Information Device Element - Type	08	08	08	08	08
221	DD	21	1		FRU Information Device Element - Revision	00	00	00	00	00
222	DE	22	1		FRU Information Device Element - Length	06	06	06	06	06
223	DF	23	1		FRU Information Device Element - SMBus/I2C Address Info	A7	A7	A7	A7	A7
224	E0	24	1		FRU Information Device Element - SMBus/I2C Capabilities	82	82	82	82	82
225	E1	25	1		FRU Information Device Element - Maximum FRU Information Device Size	08	08	08	08	08

226	E2		1	Topology MultiRecord Area	Reserved	00	00	00	00	00
227	E3		1			00	00	00	00	00
228	E4		1			00	00	00	00	00
229	E5		1			00	00	00	00	00
230	E6		1			00	00	00	00	00
231	E7		1			00	00	00	00	00
232	E8		1			00	00	00	00	00
233	E9		1			00	00	00	00	00
234	EA		1			00	00	00	00	00
235	EB		1			00	00	00	00	00
236	EC		1			00	00	00	00	00
237	ED		1			00	00	00	00	00
238	EE		1			00	00	00	00	00
239	EF		1			00	00	00	00	00
240	F0		1			00	00	00	00	00
241	F1		1			00	00	00	00	00
242	F2		1			00	00	00	00	00
243	F3		1			00	00	00	00	00
244	F4		1			00	00	00	00	00
245	F5		1			00	00	00	00	00
246	F6		1			00	00	00	00	00
247	F7		1			00	00	00	00	00
248	F8		1			00	00	00	00	00
249	F9		1			00	00	00	00	00
250	FA		1			00	00	00	00	00
251	FB		1			00	00	00	00	00
252	FC		1			00	00	00	00	00
253	FD		1			00	00	00	00	00
254	FE		1			00	00	00	00	00
255	FF		1			00	00	00	00	00

8.4 Supported Operating Systems

[Table 153] Supported Operating systems

Index	Operating Systems bootable on PM9D3a drive
1	CentOS 7.6 (Kernel 3.10.0-957)
2	CentOS 8.2 (Kernel 4.18.0-193)
3	Ubuntu 18.10 (Kernel 4.18)
4	Ubuntu 20.04 (Kernel 5.4)

9.0 PRODUCT REGULATORY COMPLIANCE

9.1 Product regulatory compliance and Certifications

Samsung SSD products comply with the following:

[Table 154] Regulations covered by region

Category	Certifications	Region or Country
EMC	CE	EU (Europe)
	UKCA	UK (without NI)
	FCC	US
	IC	Canada
	RCM	Australia & New Zealand
	Morocco	Morocco
	KC	Korea
	VCCI	Japan
	BSMI	Taiwan
Safety	c-UL-us	America (US, CANADA)
	CE	EU (Europe)
	UKCA	UK (without NI)
	TUV	-
	CB	Worldwide

Please visit the following website for additional regulatory information:
https://semiconductor.samsung.com/support/quality-support/regulatory-information/

MANUFACTURER'S DECLARATION FOR CE CERTIFICATION

Hereby, Samsung Electronics declares that the product above is in compliance with Directive 2014/30/EU, 2011/65/EU, 2014/35/EU.

EU Compliance Contact information
Samsung Electronics (UK) Ltd, Euro QA Lab, Yateley, GU46 6GG. UK

UK Conformity Assessed (UKCA)

FEDERAL COMMUNICATION COMMISSION (FCC)

This device complies with Part 15 of the FCC Rules.
Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation.

Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Responsible Party: Samsung Electronics America QA Lab
19 Chapin Rd. Building D Pine Brook NJ 07058
Tel: 1-800-SAMSUNG (1-800-726-7864)

Innovation, Science and Economic Development Canada ICES-003 Compliance
This Class B digital apparatus complies with Canadian ICES-003
Cet appareil numérique de la classe B est conforme à la norme NMB-003.
CAN ICES-3 (B)/NMB-3(B)

Korea Certification (KC)

상호 : 삼성전자㈜
기자재 명칭 : SSD
모델명 : 라벨 별도 표기
제조년월 : 라벨 별도 표기
제조자 및 제조국가 : 삼성전자㈜ / 라벨 별도 표기

Taiwan RoHS (Restriction of Hazardous Substances Directive)
若需查看更多關於 BSMI, RoHS
等的資訊，請掃描封面上的 QR 碼.


[5mm(L) × 7mm(H)]

This symbol on the product or on its packaging indicates that this product must not be disposed of with your other household waste. Instead, it is your responsibility to dispose of your waste equipment by handing it over to a designated collection point for the recycling of waste electrical and electronic equipment. The separate collection and recycling of your waste equipment at thetime of disposal will help to conserve natural resources and ensure that it is recycled in a manner that protects human health and the environment.
For more information about where you can drop off your waste equipment for recycling, please contact your local city office, your household waste disposal service, or the shop where you purchased the product.

10.0 REFERENCES

[Table 155] Standards References

Item	Website
PCI Express® Base Specification Revision 5.0	http://www.pcisig.com
PCI Express® CEM Specification Revision 5.0	http://www.pcisig.com
NVM Express™ Specification Rev. 2.0	http://www.nvmexpress.org
Enterprise SSD Form Factor Version 1.0a	http://www.ssdformfactor.org/
Solid-State Drive Requirements and Endurance Test Method (JESD218A)	http://www.jedec.org/standards-documents/docs/jesd218a
Solid-State Drive Endurance Workloads (JESD219A)	http://www.jedec.org/standards-documents/docs/jesd219a